Points missed: _____ Student's Name: _____

Total score: _____ /100 points

East Tennessee State University
Department of Computer and Information Sciences
CSCI 2150 (Tarnoff) – Computer Organization
TEST 3 for Fall Semester, 2007

Read this before starting!

- The total possible score for this test is 100 points.
- This test is ***closed book and closed notes.***
- ***Please turn off all cell phones & pagers during the test.***
- **All** answers **must** be placed in space provided. Failure to do so may result in loss of points.
- **1 point** will be deducted per answer for missing or incorrect units when required. **No** assumptions will be made for hexadecimal versus decimal, so you should always include the base in your answer.
- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.
- ***Calculators are not allowed.*** Use the tables below for any conversions you may need. Leaving an answer as a numeric expression is acceptable.

Binary	Hex
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7

Binary	Hex
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Power of 2	Equals
2^3	8
2^4	16
2^5	32
2^6	64
2^7	128
2^8	256
2^9	512
2^{10}	1 kilo (K)
2^{20}	1 mega (M)
2^{30}	1 giga (G)
2^{40}	1 tera (T)
2^{50}	1 peta (P)

"Fine print"

Academic Misconduct:

Section 5.7 "Academic Misconduct" of the East Tennessee State University Faculty Handbook, October 21, 2005:

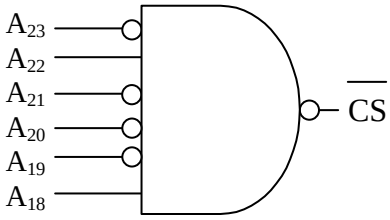
"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarism, the changing of falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of 'F' on the work in question, a grade of 'F' of the course, reprimand, probation, suspension, and expulsion. For a second academic offense the penalty is permanent expulsion."

1. For each of the following statements, place a checkmark in the column identifying which memory technology, SRAM or DRAM, the statement best describes. (1 point each)

SRAM	DRAM	
☐	☐	is made from transistors much like a D-latch
☐	☐	is typically used as cache RAM
☐	☐	is the faster of the two technologies
☐	☐	is typically used as main memory
☐	☐	needs to be refreshed/rewritten when read

2. True or false: The design of chip selects uses the same principles as that of subnet/host addressing in an IP address scheme. (2 points)

3. What are the high and low addresses (in hexadecimal) of the memory range defined with the chip select shown to the right? (4 points)



Low address: _____ High address: _____

4. For the chip select in problem 2, how big is the memory chip that uses this chip select? (3 points)

5. For the chip select in problem 2, how big is the memory space of the processor whose address lines are used for the chip select? (3 points)

6. Using logic gates, design an active low chip select for a memory device placed in a 1 Meg memory space with a low address of $D8000_{16}$ and a high address of $DBFFF_{16}$. ***Label all address lines used for chip select.*** (5 points)

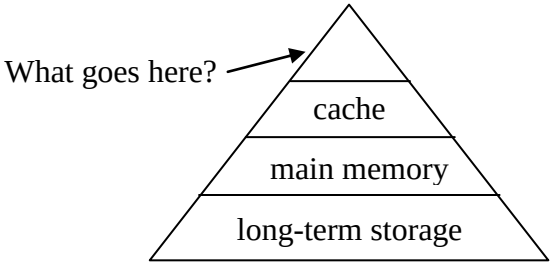
7. A chip select can have an address range from 9800_{16} to $9DFF_{16}$. (2 points)

   a.) True b.) False c.) Not enough information given

8. A chip select can be designed for a 1 Meg memory in a 16 Meg processor space where one of the memory device's addresses is $D4A1BD_{16}$. Don't try to design it; just say if it can be done. (2 points)

   a.) True b.) False c.) Not enough information given

9. The figure to the right represents the memory hierarchy with one of the levels missing. Which level is missing? (2 points)



10. Name one of the benefits of using different encoding methods to represent data on hard drive platters. (2 points)

11. True or false: It is possible to store data such that the width of 1 data bit is smaller than the width of the gap in the hard drive's write head, i.e., the minimum length of a polarity change. (2 points)

12. The average _____ is computed as the time required for the platters to make half of a revolution. (2 points)

    a.) Rotational Latency b.) Transfer time c.) Seek Time

13. _____ is the only period for which data is actually being read from the platters. (2 points)

    a.) Rotational Latency b.) Transfer time c.) Seek Time

14. The number of sectors per track on a ***constant angular velocity*** hard drive _____ as you go closer to the center of the disk. (2 points)

    a.) increases b.) decreases c.) stays the same

15. True or false: The rotational speed of the platter(s) measured in rotations per minute (RPM) of a ***multiple zone recording*** hard drive varies depending on the position of the head. (2 points)

16. Describe how the LFU replacement algorithm for the fully associative mapping algorithm works. (2 points)

17. If system's memory is to be divided into blocks of size 32, how many bits are required for the word ID? (2 points)

a.) 1 b.) 2 c.) 3 d.) 4 e.) 5 f.) cannot be determined

The table below represents a small section of a cache using fully associative mapping. Each tag and word ID is in binary while the data is in hexadecimal. Refer to it to answer questions 17 through 21.

Tag (21 bits)	Word position within block							
	000	001	010	011	100	101	110	111
110010110100110100110	00	61	C2	13	84	E5	46	A7
000110100000110010101	60	71	D2	33	94	F5	**36**	B7
010011110011011011111	20	81	E2	83	A4	05	66	C7
101110110011010100110	30	91	F2	53	B4	15	A6	D7
101001001110011010100	40	A1	02	63	C4	25	86	E7
100110100110100011001	12	34	56	78	9A	BC	DE	F0
011010110111001011001	23	45	67	89	AB	CD	EF	01
011011001101011011111	88	99	AA	BB	CC	DD	EE	FF
100010100000000010110	FE	DC	BA	98	76	54	32	10
101011001010110001101	ED	CB	A9	87	65	43	21	0F
111111010000110100110	11	44	55	77	0F	1F	2F	3F
Column →	a	b	c	d	e	f	g	h

18. Assuming the tags shown above do ***not*** delete leading zeros, how many address lines does the processor that uses this cache have? (2 points)

19. What is the block size (in number of memory locations) for the cache shown above? (2 points)

20. From what address in main memory did the value 36_{16} (the value in the second row, column g) come from? Leave your answer in binary. (2 points)

21. A copy of the data from memory address $ACAC6B_{16}$ is contained in the portion of the cache shown above. What is the value stored at that address? (3 points)

22. Name a type of instruction that would force a processor to "flush" its pipeline and begin filling it over again. (2 points)

23. Assume a pipelined processor takes 3 cycles to execute any instruction (fetch, decode, execute). How many cycles would it take to execute 6 instructions? (2 points)

24. True or false: In theory, a processor's speed can be increased by increasing the number of stages in its pipeline. (2 points)

25. What are the settings of the zero flag, sign flag, carry flag, overflow flag, and parity flag after a processor performs the addition shown to the right? (5 points)

```
  1111
  00101010
+ 01111100
  10100110
```

ZF = _____ SF = _____ CF = _____ OF = _____ PF = _____

26. The CPU has four main components. Which one performs the mathematical and logical functions, i.e., it acts as the CPU's calculator? (2 points)

27. Name one of the three purposes presented in class for a stack. (2 points)

28. Assume AX=1000_{16}, BX=2000_{16}, and CX=3000_{16}. After the following code is executed, what would AX, BX, and CX contain? (3 points)

```
PUSH AX
PUSH BX
PUSH CX
POP AX
POP BX
POP CX
```

Place your answers in space below:

AX =

BX =

CX =

29. True or false: High level languages such as C, C++, and Visual Basic have operators for performing bitwise operations. (2 points)

30. Remember that an IP address contains bits representing the subnet id and bits representing the host ID. Which bitwise operation could be used to isolate the subnet mask of an IP address, i.e., clear the bits for the host ID? (2 points)

a.) AND b.) OR c.) XOR d.) This function is not possible with a bitwise operation

31. Remember that a signed magnitude binary value represents a negative value by setting the MSB to a one. Which bitwise operation could be used to change the sign of a signed magnitude binary value, i.e., invert only the most significant bit? (2 points)

a.) AND b.) OR c.) XOR d.) This function is not possible with a bitwise operation

32. Using an original value of 10101010_2 and a mask of 00001111_2, calculate the results of a bitwise AND, a bitwise OR, and a bitwise XOR for these values. (2 points each)

Original value	Bitwise operation	Mask	Result
10101010_2	AND	00001111_2	
10101010_2	OR	00001111_2	
10101010_2	XOR	00001111_2	

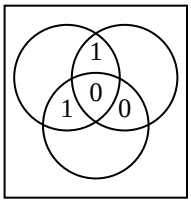
33. A CRC is calculated using a simulated long division that using a bitwise XOR instead of subtraction to generate the result. Name one of the two reasons this is done. (2 points)

34. Name two of the benefits discussed in class of serial communications over parallel. (3 points)

35. For each of the following statements, place a checkmark in the column(s) identifying which protocol(s) the statement describes. Some statements have more than one checkmark. (8 points)

Ethernet	IP	TCP	
☐	☐	☐	Used to direct packets from one device to another across multiple networks
☐	☐	☐	Uses a 7-byte preamble to synchronize all receiving devices
☐	☐	☐	Used to coordinate the breaking of a large message into smaller messages
☐	☐	☐	Uses logical addresses that are assigned to the device and can be changed
☐	☐	☐	Uses a 4-byte CRC for error checking
☐	☐	☐	Uses a 2-byte checksum for error checking that is based on the packet's header ***and*** a pseudo header created from the data and other information
☐	☐	☐	Includes a "time to live" field so that it can be removed from the network(s) in case it cannot find its destination.
☐	☐	☐	Limits the data field to a maximum of 1500 bytes

36. Add the parity/check bits that are missing from the graphic shown to the right. (2 points)



37. The graphic to the right depicts the digits of a 4-bit Hamming code where a single bit error has occurred. Circle the bit that has flipped. (2 points)