Points missed: _____ Student's Name: _____

Total score: _____/100 points

East Tennessee State University
Department of Computer and Information Sciences
CSCI 2150 (Tarnoff) – Computer Organization
TEST 3 for Spring Semester, 2007

Read this before starting!

- The total possible score for this test is 100 points.
- This test is ***closed book and closed notes.***
- ***Please turn off all cell phones & pagers during the test.***
- **All** answers **must** be placed in space provided. Failure to do so may result in loss of points.
- **1 point** will be deducted per answer for missing or incorrect units when required. **No** assumptions will be made for hexadecimal versus decimal, so you should always include the base in your answer.
- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.
- ***Calculators are not allowed.*** Use the tables below for any conversions you may need. Leaving an answer as a numeric expression is acceptable.

Binary	Hex
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7

Binary	Hex
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Power of 2	Equals
2^3	8
2^4	16
2^5	32
2^6	64
2^7	128
2^8	256
2^9	512
2^{10}	1 kilo (K)
2^{20}	1 mega (M)
2^{30}	1 giga (G)
2^{40}	1 tera (T)
2^{50}	1 peta (P)

"Fine print"

Academic Misconduct:

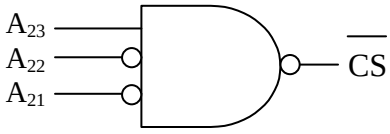
Section 5.7 "Academic Misconduct" of the East Tennessee State University Faculty Handbook, October 21, 2005:

"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarism, the changing of falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of 'F' on the work in question, a grade of 'F' of the course, reprimand, probation, suspension, and expulsion. For a second academic offense the penalty is permanent expulsion."

1. For each of the following statements, place a checkmark in the column identifying which memory technology, SRAM or DRAM, the statement best describes. (1 point each)

SRAM	DRAM	
☐	☒	is typically used as main memory
☒	☐	is typically used as cache RAM
☐	☒	is made from capacitors
☐	☒	needs to be refreshed/rewritten when read
☒	☐	is the faster of the two technologies

2. What are the high and low addresses (in hexadecimal) of the memory range defined with the chip select shown to the right? (4 points)



There are 24 address lines coming from the processor. This is determined by noting that the highest address line has a subscript of 23 and therefore, since we begin counting at 0, we know that there are 24 address lines. Address lines 21 to 23 go to the chip select circuitry while the remaining twenty-one lines, 0 through 20, go to the address inputs of the memory device.

Looking at the inputs to the NAND gate, we see that to set ^CS to zero, their values must be: A_{23}=1, A_{22}=0, and A_{21}=0. (Inverted inputs need a zero input in order to send a 1 into the NAND gate.) Therefore, the address lines have the following values for the high and low address. (Note that the shaded areas represent the bits that go into the memory device's address lines and range from all 0's for the low address to all 1's for the high address.)

Low address: $1000\ 0000\ 0000\ 0000\ 0000\ 0000_2 = 800000_{16}$
High address: $1001\ 1111\ 1111\ 1111\ 1111\ 1111_2 = 9FFFFF_{16}$

Low address: _____ High address: _____

3. For the chip select in problem 2, how big is the memory chip that uses this chip select? (3 points)

There are 21 address lines that go to the address inputs of the memory chip. Therefore, there are 2^{21} possible addresses. This means that the memory chip has $2^{21} = 2^1 \times 2^{20}$ = ***2Meg memory locations.***

4. For the chip select in problem 2, how big is the memory space of the processor whose address lines are used for the chip select? (3 points)

There are 24 address lines coming out of the processor. Therefore, there are 2^{24} possible addresses that the processor can address, i.e., the memory space is $2^{24} = 2^4 \times 2^{20}$ = ***16Meg.***

5. What is the largest memory that can have a starting address of 590000_{16}? (3 points)

Begin by converting the low address to binary. Remember that the low address must have all zeros for the address lines going to the memory chip. Therefore, the largest memory uses all of the rightmost zeros in the address.

A_{15} ↘ A_0 ↘

Low addr: $590000_{16} = 0101\ 1001\ 0000\ 0000\ 0000\ 0000_2$

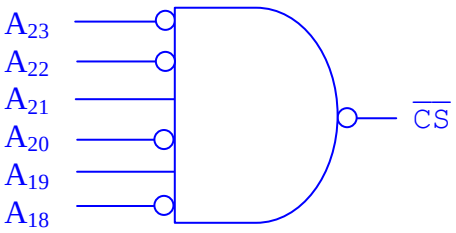
The largest memory for this address is limited to address lines A_0 through A_{15}. This means that the largest memory is limited to 16 address lines. This means that the memory chip has $2^{16} = 2^6 \times 2^{10} =$ ***64K memory locations.***

6. Using logic gates, design an active low chip select for a memory device placed in a 16 Meg memory space with a low address of 280000_{16} and a high address of $2BFFFF_{16}$. ***Label all address lines used for chip select.*** (5 points)

Since 16 Meg = $2^4 \times 2^{20} = 2^{24}$, the processor must have 24 address lines coming out of it. (A_0 through A_{23}). Converting the high and low addresses shows us where to draw the line separating the address lines that go to the chip select from the address lines that go to the memory chip.

280000_{16} = 0010 1000 0000 0000 0000 0000$_2$
$2BFFFF_{16}$ = 0010 1011 1111 1111 1111 1111$_2$

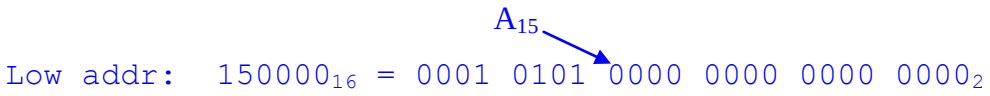
This shows that the lower 18 address lines (A_0 through A_{17}) go to the memory chip, and the upper 6 address lines (A_{18} through A_{23}) go to the chip select. Also from this diagram, we see that $A_{23} = 0$, $A_{22} = 0$, $A_{21} = 1$, $A_{20} = 0$, $A_{19} = 1$, and $A_{18} = 0$. By inverting the inputs that are to be recognized as zeros, we get the NAND circuit for the chip select shown to the right.



7. A chip select can be designed for a 128K memory device with a starting address of 150000_{16}. (2 points)

a.) True (b.) False c.) Not enough information given

Begin by converting the starting addresses to binary.



All of the address lines going to the memory chip must be set to zero for the lowest address. Since the low address 150000_{16} has contiguous zeros from bit A_0 to bit A_{15}, then all 16 of these address lines can go to the memory chip. This means that the largest memory that can start at this address is one of size $2^{16} = 2^6 \times 2^{10} = 64K$. Unfortunately, this won't be big enough, so the answer is **FALSE**.

8. A chip select can be designed for a memory device with an ending address of $35FFFF_{16}$ for a processor with a 128K memory space. (2 points)

a.) True b.) False (c.) Not enough information given

Okay, there is a problem with this. Knowing the size of the memory space of the processor is not enough to be able to identify which address lines go to the chip select NAND gate and which go to the memory device. Therefore, without knowing the size of the memory or having some other way of identifying how many address lines go to the memory, ***we do not have enough information.***

9. Name the primary characteristic of storage devices that ***improves*** as you move ***away*** from the processor toward the hard drive through the memory hierarchy? (2 points)

   The primary characteristic of storage devices that improves as you move away from the processor is capacity. Another way of saying it is that you can store much more data per dollar the farther you are from the processor.

10. By using different encoding methods, hard drive designers are able to increase _____ without changing the physical technology of the drive. (2 points)

    a.) reliability b.) data density c.) error detection d.) throughput (speed data is retrieved)
    e.) A and C f.) B and D g.) A, B, C, and D h.) C and D

11. MFM encoding has a magnetic polarity change in the middle of bit times representing logic ones and between consecutive logic zeros. This means that the width of 1 bit is equal to ____ times the width of the gap in the hard drive's write head, i.e., the minimum length of a polarity change. (2 points)

    a.) ½ b.) ¾ c.) 1 d.) 1.5 e.) 2 f.) 3 e.) varies

12. Circle ***one***: A gap is left between sectors on a hard drive. This is to: (2 points)

    a.) provide flexibility in case a new encoding algorithm is used
    b.) provide synchronization, i.e., help the hard drive controller know where the sector starts
    c.) prevent data from "bleeding over" from one track to the next.
    d.) to aid in

13. Which method of organizing hard drive sectors requires a more complex controller? (2 points)

    a.) Constant Angular Velocity b.) Multiple Zone Recording c.) Neither

14. Which method of organizing hard drive sectors allows us to achieve higher data density? (2 points)

    a.) Constant Angular Velocity b.) Multiple Zone Recording c.) Neither

15. Name one method for increasing the capacity of a hard drive. (2 points)

    Increase the number of platters
    Double sided platters
    Improved encoding
    Moving from constant angular velocity to multiple zone recording
    Smaller read/write head allowing for greater data density

16. Describe how the FIFO replacement algorithm for the fully associative mapping algorithm works. (2 points)

    The first row in is the first row deleted. Another way of saying this is that the row/block that has been in the cache the longest is the one that will be deleted if a new block needs to be loaded.

17. There were two parts to the Principle of Locality. The first was that if a piece of data or code was used once, it would most likely be used again. What was the second part? (2 points)

    Its neighboring values would most likely be needed too.

The table below represents a small section of a cache using fully associative mapping. Each tag and word ID is in binary while the data is in hexadecimal. Refer to it to answer questions 17 through 21.

Tags (binary)	Word within the block															
	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
100110100110	00	61	C2	13	84	E5	46	A7	12	34	56	78	9A	BC	DE	F0
111001011001	60	71	D2	33	94	F5	36	B7	23	45	**67**	89	AB	CD	EF	01
011011011111	20	81	E2	83	A4	05	66	C7	88	99	AA	BB	CC	DD	EE	FF
101110100110	30	91	F2	53	B4	15	A6	D7	FE	DC	BA	98	76	54	32	10
101011001100	40	A1	02	63	C4	25	86	E7	ED	CB	A9	87	65	43	21	0F
000110100110	50	B1	22	73	D4	35	96	F7	11	44	55	77	0F	1F	2F	3F
Column →	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p

18. Assuming the tags shown to the right do ***not*** delete leading zeros, how many address lines does the processor that uses this cache have? (2 points)

    In associative mapping, the tag is the same thing as the block ID. The word within the block is the same thing as the word ID. Since the full address coming from the processor consists of the block ID followed by the word ID, and since this system uses a 12 bit block ID and a 4 bit word ID, then the processor's full address is 12 + 4 = 16 bits.

19. What is the block size (in number of memory locations) for the cache shown above? (2 points)

    The size of a block is defined by the number of patterns of ones and zeros that are possible in the word ID. (Remember that the word ID defines the offset into a block.) Since this system uses a 4 bit word ID, then the size of a block is $2^4 = 16$ addresses.

20. From what address in main memory did the value 67_{16} (the value in the second row, column k) come from? Leave your answer in binary. (3 points)

    Fully associative mapping divides the physical address into two pieces, the block ID (which is used as the tag) and the word ID. In this case, the word id is the last 4 bits of the address. Since the 67_{16} has a tag of 111001011001_2 and a word id of 1010_2, then the physical address is 1110010110011010_2 **= $E59A_{16}$.**

21. A copy of the data from memory address $ACC9_{16}$ is contained in the portion of the cache shown above. What is the value stored at that address? (3 points)

    Dividing the physical address $ACC9_{16} = 1010110011001001_2$ into its tag and 4-bit word ID gives us a tag of 101011001100_2 and a word id of 1001_2. Searching through the visible lines shows us that the fifth line has the same tag, i.e., it contains the block which contains the data from the physical address $ACC9_{16}$. A word id of 1001_2 points us to the data in column j. This means that the value stored at $ACC9_{16}$ and copied into the cache is **CB_{16}.**

22. ***If*** the block containing memory address $BF16_{16}$ were to be loaded into the cache described above, which column, a, b, c, d, e, f, g, h, i, j, k, l, m, n, o, or p, would the value be loaded into? (Note: This value it is not represented in the data shown above.) (2 points)

Dividing the physical address $BF16_{16} = 1011111100010110_2$ into its tag and 4-bit word id gives us a tag of 101111110001_2 and a word id of 0110_2. The word ID of 0110_2 corresponds ***column g***.

23. Assume a processor takes 3 cycles to execute any instruction (fetch, decode, execute)

    a. How many cycles would a ***non-pipelined*** processor take to execute 4 instructions? (2 points)

A non-pipelined processor simply executes the instructions one at a time with no overlap. Therefore, the number of cycles equals 3 cycles/instruction times the number of instructions:

number of cycles = 3 × 4 = 12 cycles

    b. How many cycles would a ***pipelined*** processor take to execute 4 instructions? (2 points)

A 3-stage pipelined processor overlaps 2 cycles for each instruction as shown in the figure below.

Therefore, it will take 2 cycles to fill the pipe, then one cycle to execute each instruction. This means 2 cycles to fill the pipeline plus 4 cycles to execute the 4 instructions.

number of cycles = 2 + 4 = 6 cycles

24. What are the settings of the zero flag, the sign flag, the carry flag, the overflow flag, and the parity flag after a processor performs the addition shown to the right? (5 points)

```
1  11
  11110001
+ 10010010
  10000011
```

ZF = __**0**___ SF = __**1**___ CF = __**1**___ OF = __**0**___ PF = __**1**___

The zero flag (ZF) is set to a 1 only if the result equals 0, which in this case it does not. The sign flag (SF) is set to a one for negative values and follows the most significant bit of the result. The carry flag (CF) contains the carry out of the most significant bit of the addition. The overflow flag (OF) is set to one when there is a two's complement overflow, i.e., two positive numbers are added together resulting in a negative number or two negative numbers are added together resulting in a positive number. There is no 2's complement overflow in this addition. Lastly, the parity flag (PF) is set to a 1 if the number of ones in the resulting binary value is odd. There are three ones in the result for this case, therefore, the parity flag contains a 1.

25. Remember that a compare is basically a "virtual subtract", i.e., CMP A, B is the same thing as setting the flags after the operation A – B. What would the values of ZF and SF be ***if A is equal to B***? (2 points)

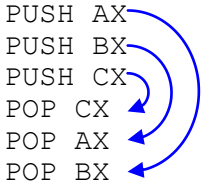
ZF = __**1**___ SF = __**0**___

A – B would result in a value of zero if A is equal to B.

26. The CPU has four main components. Three of them are the registers, the ALU, and the control unit. What is the fourth component? (2 points)

The instruction decoder

27. Assume AX=1000_{16}, BX=2000_{16}, and CX=3000_{16}. After the following code is executed, what would AX, BX, and CX contain? (3 points)



Place your answers in space below:

AX = **2000_{16}**

BX = **1000_{16}**

CX = **3000_{16}**

28. True or False: When the processor "pushes" a register to the stack, it clears the register so that it can be used for another purpose. (2 points)

FALSE: A push "copies" a value from the register to the stack without altering the value contained in the register.

29. Remember that signed binary values use the first bit as a sign bit. Which bitwise operation could be used to isolate the sign bit to tell if the number is negative, i.e., clear all bits except the MSB? (2 points)

a.) AND b.) OR c.) XOR d.) This function is not possible with a bitwise operation

30. Which bitwise operation could be used to change an even number to an odd number, i.e., force the least significant bit to a 1? (2 points)

a.) AND b.) OR c.) XOR d.) This function is not possible with a bitwise operation

31. Using an original value of 00111100_2 and a mask of 00001111_2, calculate the results of a bitwise AND, a bitwise OR, and a bitwise XOR for these values. (2 points each)

Original value	Bitwise operation	Mask	Result
00111100_2	AND	00001111_2	**00001100_2**
00111100_2	OR	00001111_2	**00111111_2**
00111100_2	XOR	00001111_2	**00110011_2**

32. A CRC is analogous to what result from what mathematical operation? Be specific. (3 points)

The remainder of a long division. The long division is simulated using a borrow-less subtract (bitwise XOR) instead of a regular subtract.

33. Name two of the benefits discussed in class of serial communications over parallel. (3 points)

- Faster communication rate due to lack of cross-talk
- Smaller connectors allowing for miniaturization
- Cheaper cabling due to fewer wires
- Fewer traces on circuit board allowing for miniaturization and cheaper circuit boards

34. The preamble of an Ethernet frame is used to: (2 points)

a.) check for errors b.) specify the header length c.) specify the data length
d.) identify the message type e.) identify the end of the frame f.) synchronize receivers

35. For each of the following statements, place a checkmark in the column(s) identifying which protocol(s) the statement describes. Some statements have more than one checkmark. (7 points)

Ethernet	IP	TCP	
☒	☐	☐	Uses a 2-byte length to identify the amount of data being transferred
☐	☒	☒	Uses a 4-bit value from which the packet header length can be calculated
☒	☐	☐	Uses addresses that are hard-wired into the network interface cards
☐	☒	☒	Uses a 2-byte checksum for error checking in the header
☒	☐	☐	Limits the data field to a maximum of 1500 bytes
☐	☒	☐	Is used to route messages across multiple networks
☐	☒	☐	Includes a “time to live” field so that it can be removed from the network(s) in case it cannot find its destination.