Points missed: _____ Student's Name: _____

Total score: _____ /100 points

East Tennessee State University
Department of Computer and Information Sciences
CSCI 2150 (Tarnoff) – Computer Organization
TEST 3 for Spring Semester, 2009

Read this before starting!

- The total possible score for this test is 100 points.
- All problems are worth 2 points unless otherwise noted.
- This test is ***closed book and closed notes.***
- ***Please turn off all cell phones & pagers during the test.***
- **All** answers **must** be placed in space provided. Failure to do so may result in loss of points.
- **1 point** will be deducted per answer for missing or incorrect units when required. **No** assumptions will be made for hexadecimal versus decimal, so you should always include the base in your answer.
- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.
- ***Calculators are not allowed.*** Use the tables below for any conversions you may need. Leaving an answer as a numeric expression is acceptable.

Binary	Hex
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7

Binary	Hex
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Power of 2	Equals
2^3	8
2^4	16
2^5	32
2^6	64
2^7	128
2^8	256
2^9	512
2^{10}	1 kilo (K)
2^{20}	1 mega (M)
2^{30}	1 giga (G)
2^{40}	1 tera (T)
2^{50}	1 peta (P)

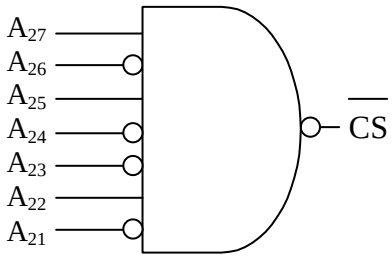
"Fine print"

Academic Misconduct:

Section 5.7 "Academic Misconduct" of the East Tennessee State University Faculty Handbook, October 21, 2005:

"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarism, the changing of falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of 'F' on the work in question, a grade of 'F' of the course, reprimand, probation, suspension, and expulsion. For a second academic offense the penalty is permanent expulsion."

1. True or false: All memory devices connected to a processor's system bus must be the same size due to chip select circuitry constraints. (1 point)
2. How many 1-bit storage cells, e.g., D-latches, are contained in a memory that has 16 address lines and 8 data lines?
3. What are the high and low addresses ***in hexadecimal*** of the memory range defined with the chip select shown to the right? (4 points)



Low address: _____ High address: _____

4. For the chip select in problem 3, how big is the memory chip that uses this chip select? (3 points)
5. For the chip select in problem 3, how big is the memory space of the processor whose address lines are used for the chip select? (3 points)
6. Using logic gates, design an active low chip select for a memory device placed in a ***4 Meg*** memory space with a low address of $3C0000_{16}$ and a high address of $3DFFFF_{16}$. ***Label all address lines used for chip select.*** (5 points)
7. A 16K memory can have a starting (lowest) address of $93C000_{16}$ in a processor's memory space.

   a.) True b.) False c.) Not enough information given

8. A chip select circuit for a single memory device can be designed for the address range $5D000_{16}$ to $5EFFF_{16}$.

   a.) True b.) False c.) Not enough information given

9. A chip select circuit for a 256K memory device placed inside of a 1 Meg processor memory space can be designed knowing only that one of the addresses inside of its range is 43564_{16}.

   a.) True b.) False c.) Not enough information given

10. Name a characteristic of memory that ***improves*** as you move down in the memory hierarchy, i.e., father from the processor.

11. Identify ***all*** of the following statements that are true regarding a hard drive's read/write head? (3 points)

    a.) The farther a hard drive's write head is from the platters, the larger the write head gap must be in order to reliably write to the disks.

    b.) For a specific encoding method, the minimum space reserved for a single bit on a hard drive is directly proportional to the gap in the write head.

    c.) By modifying the hard drive controller to use a different encoding method, the data density on the platters can be increased with no modification to the write head or the platters.

    d.) A Winchester head was developed to have the head float on a cushion of air so that it keeps a more consistent distance from the hard drive's platters.

12. Which one of the following measurements used to calculate hard drive data access times is most accurately predictable?

    a.) queuing time b.) rotational latency c.) transfer time d.) seek time

13. The time to read a fragmented file from a hard drive is greatly increased over a non-fragmented file because of the numerous delays due to _____. Circle all that apply.

    a.) queuing time b.) rotational latency c.) transfer time d.) seek time

14. The speed at which the data is read from the platters of a ***multiple zone recording*** hard drive _____ as you go toward the outside tracks of a hard disk.

    a.) increases b.) decreases c.) stays the same d.) cannot be predicted

15. True or false: One drawback of ***multiple zone recording*** hard drives is that they require more complex controllers capable of much higher data rates. (1 point)

16. If the word ID used by the cache of a processor with a 1 Gig memory space uses 3 bits, then the number of words in a block equals _____?

a.) 2^2 b.) 2^3 c.) 2^4 d.) 2^{27} e.) 2^{30} f.) cannot be determined

The table below represents a small section of a cache using fully associative mapping. Each tag and word ID is in binary while the data is in hexadecimal. Refer to it to answer questions 16 through 19.

Tags (binary)	Word within the block															
	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
1100011111010000	00	61	C2	13	84	E5	46	A7	12	34	56	78	9A	BC	DE	F0
0101100110001110	60	71	D2	33	94	F5	36	B7	23	45	67	89	AB	CD	EF	01
1101001101000011	20	81	E2	83	A4	05	66	C7	88	99	AA	BB	CC	DD	EE	FF
0101100111100110	30	91	F2	53	B4	15	A6	D7	FE	DC	BA	98	76	54	32	10
1001011011010110	40	A1	02	63	C4	25	86	E7	ED	CB	**A9**	87	65	43	21	0F
1101100011011001	50	B1	22	73	D4	35	96	F7	11	44	55	77	0F	1F	2F	3F
Column →	a	b	c	d	e	f	g	h	i	j	k	l	M	n	o	p

17. Assuming the tags shown above do ***not*** delete leading zeros, how many address lines does the processor that uses this cache have?

18. How many word ID bits does this cache use to define a block size?

19. From what address in main memory did the value $A9_{16}$ (the value in the fifth row, column k) come from? Leave your answer in binary.

20. A copy of the data from main memory address $D3438_{16}$ is contained in the portion of the cache shown above. What is the value stored at that address? (3 points)

21. Which of the following statements are true regarding the relationship between a processor's L1 and L2 caches? Circle all that apply. (4 points)

a.) One of them contains code while the other contains data.
b.) L1 is smaller and faster than L2
c.) L1 is always inside the processor chip while L2 may or may not be inside the processor chip.
d.) Blocks contained in L1 must also be contained in L2.

22. When trying to load a new block into a fully associative cache that is full, the FIFO cache replacement algorithm replaces the block in the cache that has been in the cache the longest. What is one of the drawbacks of this type of replacement algorithm? (3 points)

23. What is the most common reason for a processor's instruction pipeline to be flushed?

24. Assume a processor takes 3 cycles to execute any instruction (fetch, decode, execute)

a. How many cycles would a ***non-pipelined*** processor take to execute 9 instructions? (2 points)

b. How many cycles would a ***pipelined*** processor take to execute 9 instructions? (2 points)

25. What are the settings of the zero flag, sign flag, carry flag, overflow flag, and parity flag after a processor performs the addition shown to the right? Remember to treat the parity flag as the Intel x86 processors would. (5 points)

```
  1  11111
     10110101
+    11111100
    10110001
```

ZF = _____ SF = _____ CF = _____ OF = _____ PF = _____

26. Which of the following four components of the CPU ***does not*** have a direct connection to the CPU's internal data bus. (Select only one.)

a.) Control Unit b.) Registers c.) Instruction Decoder d.) ALU

27. Assume AX=1000_{16}, BX=2000_{16}, and CX=3000_{16}. After the following code is executed, what would AX, BX, and CX contain? (3 points)

Place your answers in space below:

```
PUSH AX
PUSH BX
PUSH CX
POP AX
POP CX
POP BX
```

AX =

BX =

CX =

28. Three uses were discussed in class for the stack. Describe one.

29. Assume we want to take the negative of an 8-bit signed magnitude value by inverting the most significant bit (the sign bit). Which bitwise operation could be used to do this?

a.) AND b.) OR c.) XOR d.) This function is not possible with a bitwise operation

30. What would the mask look like for the previous problem?

a.) 10000000_2 b.) 01111111_2 c.) As I said before, this function isn't possible

31. Using an original value of 11000011_2 and a mask of 11110000_2, calculate the results of a bitwise AND, a bitwise OR, and a bitwise XOR for these values. (2 points each)

Original value	Bitwise operation	Mask	Result
11000011_2	AND	11110000_2	
11000011_2	OR	11110000_2	
11000011_2	XOR	11110000_2	

32. There were two reasons given in class for using a "borrow-less" subtraction to simulate a long division when generating a CRC. Name one.

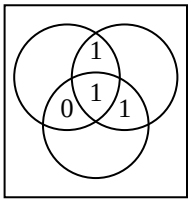
33. The borrow-less subtraction is performed using which bitwise operation?

a.) AND b.) OR c.) XOR d.) This function is not performed with a bitwise operation

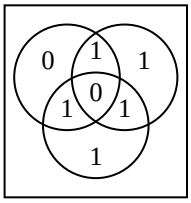
34. For each of the following statements, place a checkmark in the column(s) identifying which protocol(s) the statement describes. Some statements have more than one checkmark. (8 points)

Ethernet	IP	TCP	
☐	☐	☐	Has a preamble to synchronize the receiving network interface cards (NICs)
☐	☐	☐	Uses 6-byte MAC addresses to uniquely identify NICs on the network
☐	☐	☐	Uses a CRC to check for errors across the whole frame
☐	☐	☐	Identifies the packet's purpose by using ports such as port 80 (http)
☐	☐	☐	Uses 4-byte logical addresses instead of physical addresses (Version 4)

35. Add the parity/check bits that are missing from the graphic shown to the right.



36. The graphic to the right depicts the digits of a 4 data-bit/3 check-bit Hamming code where a single bit error has occurred. Circle the bit that has flipped.



37. Which of the following does the graphic to the right depict?

a.) No error
b.) A single bit error
c.) Double bit errors