Points missed: _____ Student's Name: _____

Total score: _____/100 points

East Tennessee State University
Department of Computer and Information Sciences
CSCI 2150 (Tarnoff) – Computer Organization
TEST 2 for Fall Semester, 2007

Read this before starting!

- The total possible score for this test is 100 points.
- This test is ***closed book and closed notes.***
- ***Please turn off all cell phones & pagers during the test.***
- **All** answers **must** be placed in space provided. Failure to do so may result in loss of points.
- **1 point** will be deducted per answer for missing or incorrect units when required. **No** assumptions will be made for hexadecimal versus decimal, so you should always include the base in your answer.
- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.
- ***Calculators are not allowed.*** Use the tables below for any conversions you may need. Leaving numeric equations is fine too.

Binary	Hex
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7

Binary	Hex
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Power of 2	Equals
2^3	8
2^4	16
2^5	32
2^6	64
2^7	128
2^8	256
2^9	512
2^{10}	1K
2^{20}	1M
2^{30}	1G

"Fine print"

Academic Misconduct:

Section 5.7 "Academic Misconduct" of the East Tennessee State University Faculty Handbook, June 1, 2001:

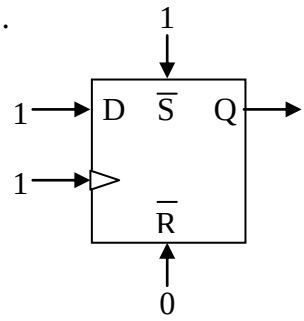
"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarism, the changing of falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of 'F' on the work in question, a grade of 'F' of the course, reprimand, probation, suspension, and expulsion. For a second academic offense the penalty is permanent expulsion."

Short answers – 2 points each unless otherwise noted

For the following ***three*** circuits, identify the value of the output Q from the following choices. Consider the D-latch a ***rising edge triggered latch***.

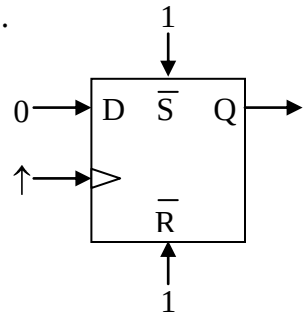
a.) 1 b.) 0 c.) Q_0 (stored value of Q) d.) undefined/illegal e.) can't tell

1.



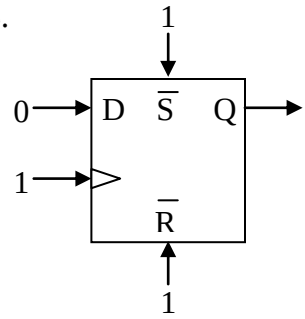
Answer: b
The R-bar line is low which overrides any D or clock input. R-bar when asserted forces the output to equal 0. Therefore, the answer is b.

2.



Answer: b
Both R-bar and S-bar are high which mean they have no affect on the output Q. That means we need to examine the clock to see if it is affecting the output. The clock is rising, therefore, it is copying D to Q. Since D equals 0, then Q equals 0.

3.



Answer: c
Both R-bar and S-bar are high which mean they have no affect on the output Q. That means we need to examine the clock to see if it is affecting the output. The clock is high, so it is ***not*** copying D to Q. Therefore, the old value of Q is still stored on Q.

4. True or False: The expression $A \cdot B \cdot C + \overline{A} + A \cdot \overline{B} \cdot \overline{C}$ is in correct Sum-of-Products format.

TRUE: The only thing remotely odd about this expression is the lone A-bar term. This isn't a problem as far as being considered a stand-alone product to be OR'ed with the other products.

5. The expression $\overline{A} \cdot B \cdot C + A \cdot B \cdot C + \overline{A \cdot B}$ is not in proper Sum-of-Products format. What boolean algebra operation would you need to apply first to correct this?

a.) It's not a problem; illegal term drops out b.) Distributive Law c.) Use "F-O-I-L"
d.) Take the inverse of the inverse e.) DeMorgan's Theorem f.) It can't be fixed

The problem is the bar across the two terms of the final product. The inverse needs to be distributed to both of the inputs. The only way to distribute a bar is with DeMorgan's Theorem.

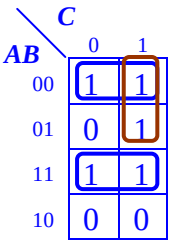
6. How many cells would a four-input Karnaugh Map have?

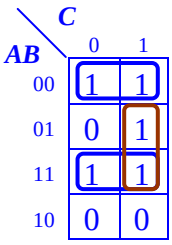
   a.) 2 b.) 4 c.) 6 d.) 8 e.) 12 f.) 16 g.) 32

   There are $2^4 = 16$ possible combinations of 1's and 0's for four inputs. Therefore, since the Karnaugh map must have one cell for each combination just like a truth table must have one row for each combination, there are 16 cells.

7. True or False: If it has been properly done, there is only one way to arrange the rectangles in a Karnaugh map for a specific pattern of 1's and 0's.

   FALSE: The best way to show this statement is false is to give you an example. The following K-maps have the same pattern of ones and zeros, but different rectangles (both correct) to cover them.

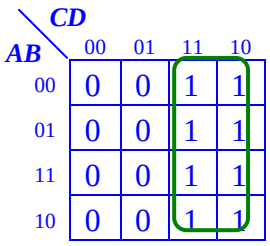




8. In a 4-variable Karnaugh map, how many input variables (A, B, C, and/or D) does a single product have if its corresponding rectangle of 1's contains 8 cells?

   a.) 1 b.) 2 c.) 3 d.) Cannot be determined

   The simplest way to answer this question is to create a 4-variable/input Karnaugh map that has a rectangle with eight 1's, then figure out what the product is. The number of inputs in the product will give us our answer.



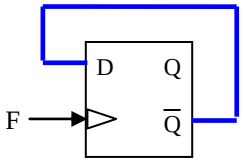
A	B	C	D	
0	0	1	1	
0	0	1	0	
0	1	1	1	
0	1	1	0	C
1	1	1	1	
1	1	1	0	
1	0	1	1	
1	0	1	0	

   The resulting product has a single input, C. You'll find that regardless of how the 8 cell rectangle is arranged, the resulting product will always have 1 input.

9. An active-low transparent latch copies data from the D input to the Q output when the clock is:

   a.) a logic 0 c.) changing from a 1 to a 0 b.) a logic 1 d.) changing from a 0 to a 1

10. Make the connections to the latch in the figure to the right that makes a divide-by-two circuit, i.e., divides the frequency F in half at the output Q.



11. Which of the following expressions produces the truth table to the right?

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

a.) $A \cdot \overline{B} + C$ b.) $A + C$ c.) $A \cdot B + C$

d.) $B + C$ e.) $A + \overline{B} \cdot C$ f.) $\overline{A} + \overline{B} \cdot C$

The answer keys for the previous tests show a number of ways to solve this problem. I still think the easiest way to do this is to simply put together the truth table for each of the options a through f to see if any of them match. For example, $A \cdot \overline{B} + C$ is equal to 1 when $A \cdot \overline{B}$ equals 1 (A=1 and B=0) or when C equals 1. This gives us a truth table with a 1 in the following rows:

A=1, B=0, C=0 A=1, B=0, C=1

A=0, B=0, C=1 A=0, B=1, C=1 A=1, B=0, C=1 A=1, B=1, C=1

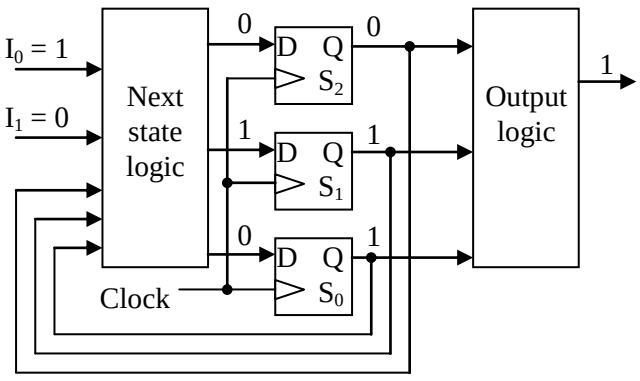
The first two are for A=1 and B=0 while the last 4 represent when C=1. All other rows will be 0.

If we do this for all options a through f, we get the following truth tables. Column a equals 1 only when A=1 and B=0 or when C=1. Column b equals 1 when A=1 or when C=1. Column c equals 1 when A=1 and B=1 or when C=1. Column d equals 1 when B=1 or when C=1. Column e equals 1 when A=1 or when B=0 and C=1. Column f equals 1 when A=0 or when B=0 and C=1. The only column that matches the original truth table exactly is column f. Therefore, the answer is f.

A	B	C	a	b	c	d	e	f
0	0	0	0	0	0	0	0	1
0	0	1	1	1	1	1	1	1
0	1	0	0	0	0	1	0	1
0	1	1	1	1	1	1	0	1
1	0	0	1	1	0	0	1	0
1	0	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	0
1	1	1	1	1	1	1	1	0

Another way to look at this (and very quickly answer the question) is that the only option from the list of choices where the top row can possibly equal 1 (A=0, B=0, and C=0) is choice f. All other choices must have at least one of the inputs equal to 1 in order to output a 1.

The next six problems use the state machine circuit to the right. Assume that the states are numbered so that bit S_2 is the most significant bit and bit S_0 is the least significant bit.



12. What is the maximum number of states that this system can handle?

Since there are three latches, then the internal memory of this state machine can remember $2^3 = 8$ states: 000, 001, 010, 011, 100, 101, 110, and 111. Therefore, the answer is 8.

13. What is the current state of this system? Keep your answer in binary.

The current state is the value stored in the three latches and found at the Q outputs. In the case of the diagram above, that is 011 with S_2 being used as the most significant bit.

14. If the clock were to pulse right now, what would the next state be? Keep your answer in binary.

The next state is the value present at the D inputs, i.e., the value that would be stored if we had a clock pulse occur. In the case of the diagram above, that is 010 with S_2 being the most significant bit.

15. The truth table to the right represents the output logic truth table for the above state machine. Circle the row that identifies the current output condition of the system, i.e., which row is represented by the state of the logic in the diagram above?

S_2	S_1	S_0	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

The output is determined by the current state, i.e., 011. Therefore, the third row identifies the output, which matches the 1 output from the figure.

16. If the clock were to pulse right now, what would the new output be? Use the truth table from the previous problem to answer the question.

a.) 0 b.) 1 c.) Not enough information given

Since the next state is 010, we go to the row in the truth table for 010. This shows us that the output for the next state is 0.

17. How many rows would the next state logic truth table have for this circuit?

a.) $2^2 = 4$ b.) $2^3 = 8$ c.) $2^4 = 16$ d.) $2^5 = 32$ e.) $2^6 = 64$

Remember that the next state logic truth table depends on the current state (derived from S_2, S_1, and S_0) and the current input (I_1 and I_0). This gives us 5 inputs. Since there are $2^5 = 64$ combinations of 1's and 0's for 5 inputs, the answer is d. (Counting the arrows into the block labeled "Next state logic" would have also shown that there are 5 inputs to this logic.)

18. True or False: Re-numbering the states of a state machine has no effect on the "next state" logic for the digital hardware implementation.

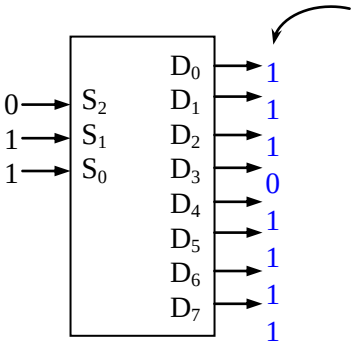
The numbering of the states directly affects the next state truth table, and therefore changes the logic that is derived from it. Therefore, the answer is **False**.

19. How many latches will a state machine with 128 states require?

a.) 3 b.) 4 c.) 5 d.) 6 e.) 7 f.) 8 g.) 9

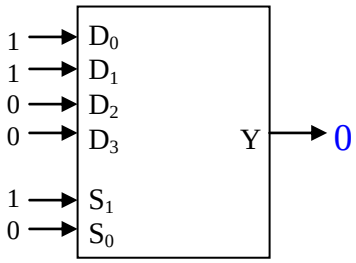
With 128 states, they would be numbered 0, 1, 2, 3, … , and 127. Since $127_{10} = 1111111_2$, we will need 7 bits to represent the state. **Therefore, the answer is e.** Another way of looking at it is to see how many states it is possible to represent with n bits, and to figure out what value of 2^n is greater than or equal to 128 different values. $2^5 = 32$ which is not enough, $2^6=64$ which is still not enough, but $2^7=128$ is exactly enough. Therefore, 7 bits will do the trick.

20. For the ***active-low*** output decoder shown to the right, fill in the values for all of the outputs D_0 through D_7. Assume S_2 is most significant bit of the inputs. (3 points)



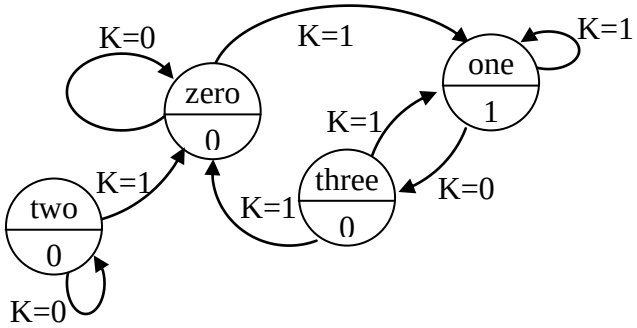
Remember that the bits S_2, S_1, and S_0 make up a digital selector with S_2 being the most significant bit. The digital value of these three bits is 011 which when converted to decimal gives us 3. That means that output D_3, the emphasis being placed on the 3, is the selected output.

21. For the multiplexer/selector shown to the right, what is the output Y?



Similar to the previous problem, the output is "selected" by the selector inputs S_1 and S_0 with S_1 being the most significant bit. The digital value of these two bits is 10_2 which equals a decimal 2. Therefore, the input D_2 is going to be routed to the output Y making Y have an output of 0.

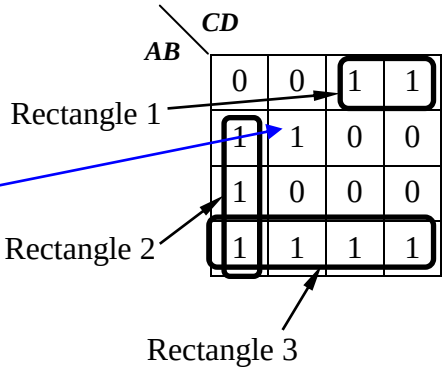
22. Identify the two errors in the state diagram to the right. The circuit is to have a single binary input K. Do not bother to correct the errors. (2 points for each error identified correctly)



The first problem is that there is no way to get to state "two". Okay, there is an arrow going into state two, but it is from itself which still means that there is no way to get from any state to state two.

The second problem is that state "three" has two transitions leaving it for when K=1 (a problem in itself), and no transition for K=0.

23. For the Karnaugh map to the right, identify three ***problems*** with how the rectangles have been made. Note that not all of the problems may be with a specific rectangle, but if there is a problem with a rectangle, be sure to identify it using the names given. (2 points each)



Problem 1: There is a 1 that is not covered by any rectangle.

Problem 2: Rectangle 2 contains three cells which is not a power of two.

Problem 3: Rectangle 1 isn't as large as it could be. It could cross the top/bottom borders to include the two, rightmost ones in Rectangle 3.

Medium answers – 4 points each

24. Complete the truth table to the right with the values for the following sum-of-products expression:

$$C + \overline{A} \cdot B$$

A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Remember that each product generates a 1 when all of its inputs are one, e.g., $1 \cdot 1 \cdot 1 = 1$. This means that if we can figure out where each product equals one, we know where the ones are in the truth table. The remaining positions are filled with zeros.

The first product, C, equals one when C=1. Therefore, all rows where C=1 should be set to 1.

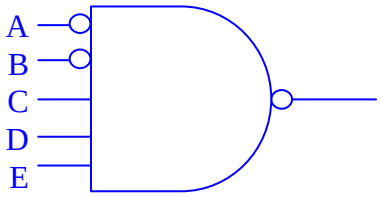
The second product, $\overline{A} \cdot B$, equals 1 when A=0 and when B=1. This happens in the third and fourth rows of the truth table. This gives us the pattern of ones and zeros you see filled in above.

25. In the Karnaugh map to the right, draw the best pattern of rectangles you can. ***Do not derive the SOP expression.***

Remember to only include X's in rectangles if they make the rectangle bigger. Do not include an X if it adds an additional rectangle.

AB \ CD	00	01	11	10
00	1	0	0	0
01	1	0	0	0
11	X	X	X	0
10	0	1	1	1

26. In the space to the right, draw the decoding logic circuit with an active-low output that identifies when A = 0, B = 0, C = 1, D = 1, and E = 1.

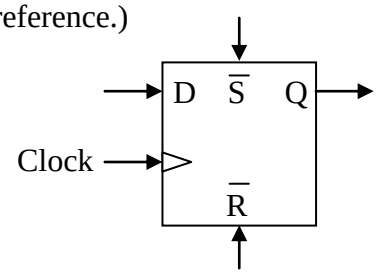


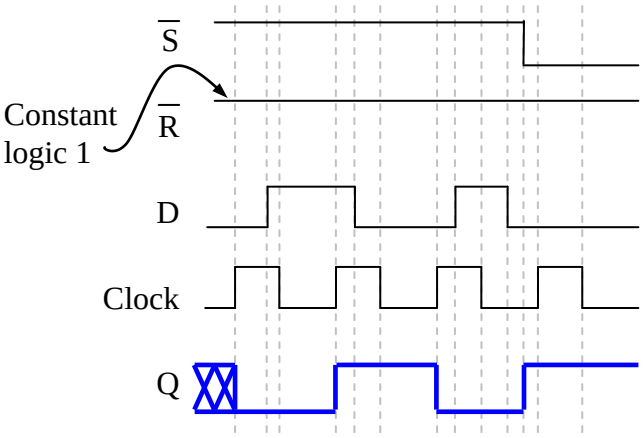
27. Create a Karnaugh map from the truth table below. ***Do not worry about making the rectangles.***

A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

AB \ C	0	1
00	0	1
01	1	0
11	1	0
10	0	1

28. Show the *D* latch output waveform *Q* based on the inputs *D*, $\overline{S}$, $\overline{R}$, and clock indicated in the graph to the right. Assume the latch captures on the rising edge. (The figure below is just for a reference.)





First of all, since both S-bar and R-bar are 1 when the timing diagram first starts, we don't have an initial state for Q. That's why I put the hash marks. It isn't until the first rising edge on the clock when D=0 is copied to Q that we know what Q equals. After that, every time we get a rising edge on the clock, D is copied to Q. That is until S-bar goes to zero. This forces Q to 1 and makes it so that the clock pulses are ignored.

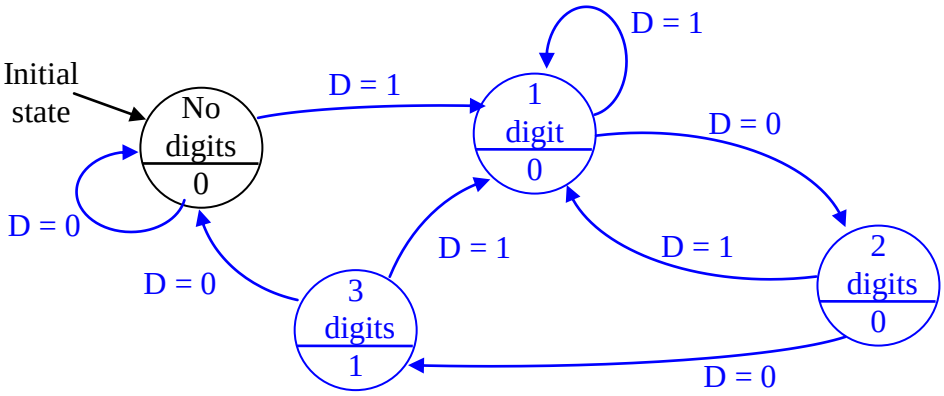
Longer answers – Points vary per problem

29. Make the state diagram that will output a '1' when the sequence '100' is detected in a serial stream of bits. For example, if the following binary stream is received:

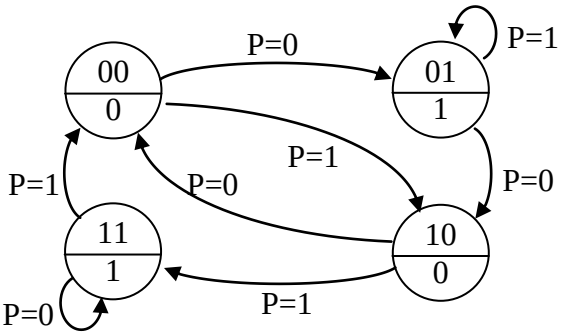
1 0 1 0 1 1 1 0 1 0 0 1 0 1 1 0 0 0 1 1 0 1 1 1 0 0 1 0

then 1's will be output at these points. At all other times, the system will output zeros. Label the input D. (7 points)

There are some things to note about this figure. First, the four states represent the four conditions of having no bits, having 1 bit, having 2 bits, and having all bits. The output equals 1 only when all bits have been received. Second, since the sequence starts with a 1 and there is only a single one in the sequence, then any time the input equals 1, the system is supposed to go to the "got first bit" state (i.e., "1 digit" state). After receiving a 1, the only way to get to the "3 digits" state is to receive two zeros in sequence after receiving the starting 1 bit.



30. Create the next state truth table and the output truth table for the state diagram to the right. The states have already been numbered. Use the variable names S_1 and S_0 to represent the most significant and least significant bits respectively of the binary number identifying the state. Label the output 'X'. (7 points)



Next State T.T.

S_1	S_0	P	S_1'	S_0'
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	0	0
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

Output T.T.

S_1	S_0	X
0	0	0
0	1	1
1	0	0
1	1	1

31. Derive the minimum SOP expression from the Karnaugh map below. (6 points)

AB \ CD	00	01	11	10
00	0	0	1	0
01	0	1	1	1
11	0	0	1	1
10	0	0	1	0

Red rectangle

A	B	C	D
0	1	1	1
0	1	1	0
1	1	1	1
1	1	1	0

A and D drop out. Since both B and C equal 1 for all cells, neither is inverted.

$B \cdot C$

Blue rectangle

A	B	C	D
0	0	1	1
0	1	1	1
1	1	1	1
1	0	1	1

A and B drop out. Since both C and D equal 1 for all cells, neither is inverted.

$C \cdot D$

Green rectangle

A	B	C	D
0	1	0	1
0	1	1	1

C is the only term to drop out. Of the remaining inputs, only A is 0 for all cells, so it is inverted.

$\overline{A} \cdot B \cdot D$

The final answer is:

$B \cdot C + C \cdot D + \overline{A} \cdot B \cdot D$

32. The three Boolean expressions below represent the ***next state bits (S_0' and S_1')*** and the ***output bit X*** based on the ***current state (S_0 and S_1)*** and the ***input A***. Draw the logic circuit for the state machine including the latches and output circuitry. ***Be sure to label the latch inputs and other signals.*** (7 points)

$S_0' = \overline{A}$ $\qquad$ $S_1' = S_0 + S_1$ $\qquad$ $X = \overline{S_1 \cdot S_0}$