Points missed: _____   Student's Name: _____

Total score: _____/100 points

East Tennessee State University
Department of Computer and Information Sciences
CSCI 2150 (Tarnoff) – Computer Organization
TEST 2 for Fall Semester, 2007

Read this before starting!

- The total possible score for this test is 100 points.
- This test is ***closed book and closed notes.***
- ***Please turn off all cell phones & pagers during the test.***
- **All** answers **must** be placed in space provided. Failure to do so may result in loss of points.
- **1 point** will be deducted per answer for missing or incorrect units when required. **No** assumptions will be made for hexadecimal versus decimal, so you should always include the base in your answer.
- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.
- ***Calculators are not allowed.*** Use the tables below for any conversions you may need. Leaving numeric equations is fine too.

| Binary	Hex		Binary	Hex		Power of 2	Equals
0000	0		1000	8		2^3	8
0001	1		1001	9		2^4	16
0010	2		1010	A		2^5	32
0011	3		1011	B		2^6	64
0100	4		1100	C		2^7	128
0101	5		1101	D		2^8	256
0110	6		1110	E		2^9	512
0111	7		1111	F		2^{10}	1K
						2^{20}	1M
						2^{30}	1G

"Fine print"

For the following ***three*** circuits, identify the value of the output Q from the following choices. Consider the D-latch a ***rising edge triggered latch***.

a.) 1   b.) 0   c.) Q_0 (stored value of Q)   d.) undefined/illegal   e.) can't tell

1.   Answer: _____   2.   Answer: _____   3.   Answer: _____
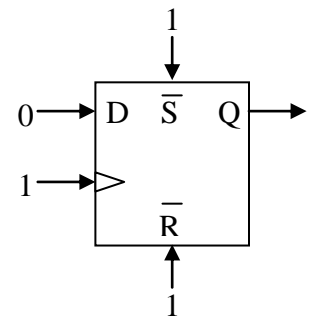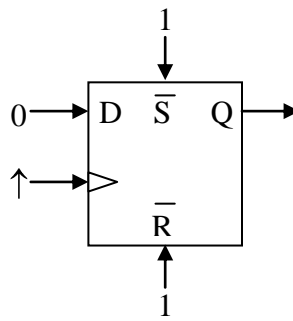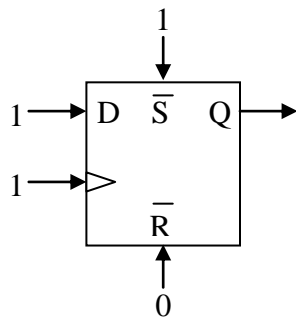
4. True or False: The expression $A \cdot B \cdot C + \overline{A} + A \cdot \overline{B} \cdot \overline{C}$ is in correct Sum-of-Products format.

5. The expression $\overline{A \cdot B \cdot C} + A \cdot B \cdot C + \overline{A \cdot B}$ is not in proper Sum-of-Products format. What boolean algebra operation would you need to apply first to correct this?

    a.) It's not a problem; illegal term drops out   b.) Distributive Law   c.) Use "F-O-I-L"
    d.) Take the inverse of the inverse   e.) DeMorgan's Theorem   f.) It can't be fixed

6. How many cells would a four-input Karnaugh Map have?

    a.) 2   b.) 4   c.) 6   d.) 8   e.) 12   f.) 16   g.) 32

7. True or False: If it has been properly done, there is only one way to arrange the rectangles in a Karnaugh map for a specific pattern of 1's and 0's.

8. In a 4-variable Karnaugh map, how many input variables (A, B, C, and/or D) does a single product have if its corresponding rectangle of 1's contains 8 cells?

    a.) 1   b.) 2   c.) 3   d.) Cannot be determined

9. An active-low transparent latch copies data from the D input to the Q output when the clock is:

    a.) a logic 0   c.) changing from a 1 to a 0   b.) a logic 1   d.) changing from a 0 to a 1

10. Make the connections to the latch in the figure to the right that makes a divide-by-two circuit, i.e., divides the frequency F in half at the output Q.
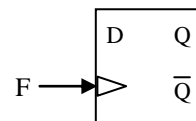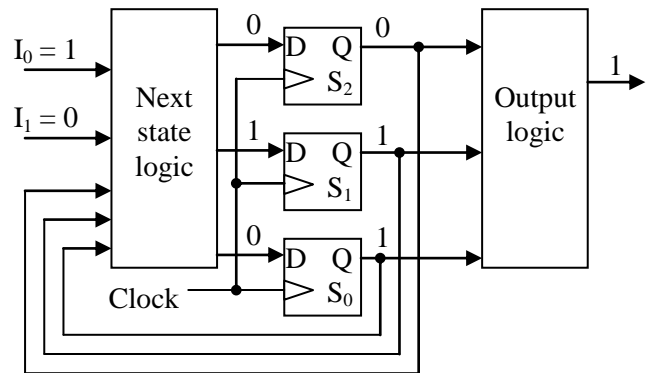
11. Which of the following expressions produces the truth table to the right?

a.) $A \cdot \bar{B} + C$ b.) $A + C$ c.) $A \cdot B + C$

d.) $B + C$ e.) $A + \bar{B} \cdot C$ f.) $\bar{A} + \bar{B} \cdot C$

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

The next six problems use the state machine circuit to the right. Assume that the states are numbered so that bit S_2 is the most significant bit and bit S_0 is the least significant bit.

12. What is the maximum number of states that this system can handle?

13. What is the current state of this system? Keep your answer in binary.

14. If the clock were to pulse right now, what would the next state be? Keep your answer in binary.

15. The truth table to the right represents the output logic truth table for the above state machine. Circle the row that identifies the current output condition of the system, i.e., which row is represented by the state of the logic in the diagram above?

S_2	S_1	S_0	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

16. If the clock were to pulse right now, what would the new output be? Use the truth table from the previous problem to answer the question.

a.) 0 b.) 1 c.) Not enough information given

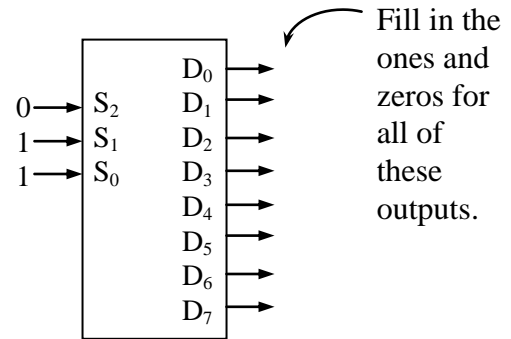17. How many rows would the next state logic truth table have for this circuit?

a.) $2^2 = 4$ b.) $2^3 = 8$ c.) $2^4 = 16$ d.) $2^5 = 32$ e.) $2^6 = 64$

18. True or False: Re-numbering the states of a state machine has no effect on the "next state" logic for the digital hardware implementation.
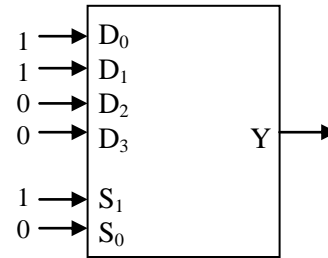
19. How many latches will a state machine with 128 states require?

a.) 3 b.) 4 c.) 5 d.) 6 e.) 7 f.) 8 g.) 9

20. For the *active-low* output decoder shown to the right, fill in the values for all of the outputs D_0 through D_7. Assume S_2 is most significant bit of the inputs. (3 points)


Fill in the ones and zeros for all of these outputs.

$0 \longrightarrow S_2$
$1 \longrightarrow S_1$
$1 \longrightarrow S_0$

D_0
D_1
D_2
D_3
D_4
D_5
D_6
D_7

21. For the multiplexer/selector shown to the right, what is the output Y?

$1 \longrightarrow D_0$
$1 \longrightarrow D_1$
$0 \longrightarrow D_2$
$0 \longrightarrow D_3$

$1 \longrightarrow S_1$
$0 \longrightarrow S_0$

Y

22. Identify the two errors in the state diagram to the right. The circuit is to have a single binary input K. Do not bother to correct the errors. (2 points for each error identified correctly)

K=0   K=1   K=1
one
zero
0   K=1   1
K=1
two   three   K=0
0   K=1   0
K=0
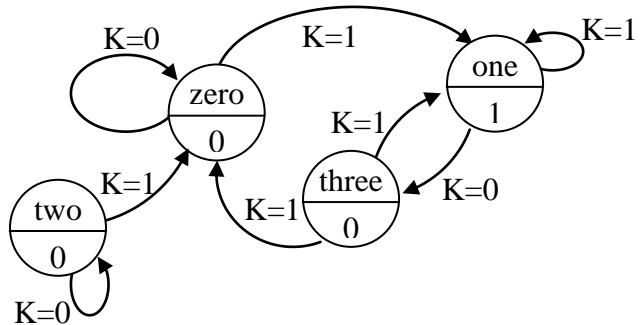
23. For the Karnaugh map to the right, identify three *problems* with how the rectangles have been made. Note that not all of the problems may be with a specific rectangle, but if there is a problem with a rectangle, be sure to identify it using the names given. (2 points each)
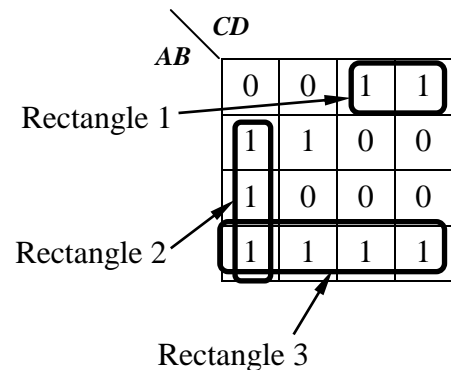
Problem 1:

Problem 2:

Problem 3:

CD
AB

Rectangle 1

0	0	1	1
1	1	0	0
1	0	0	0
1	1	1	1

Rectangle 2

Rectangle 3

24. Complete the truth table to the right with the values for the following sum-of-products expression:

$$C + \overline{A} \cdot B$$

A	B	C	X
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

25. In the Karnaugh map to the right, draw the best pattern of rectangles you can. ***Do not derive the SOP expression.***

	CD 00	01	11	10
AB 00	1	0	0	0
01	1	0	0	0
11	X	X	X	0
10	0	1	1	1

26. In the space to the right, draw the decoding logic circuit with an active-low output that identifies when A = 0, B = 0, C = 1, D = 1, and E = 1.

27. Create a Karnaugh map from the truth table below. ***Do not worry about making the rectangles.***

A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

28. Show the *D* latch output waveform *Q* based on the inputs *D*, $\overline{S}$, $\overline{R}$, and clock indicated in the graph to the right. Assume the latch captures on the rising edge. (The figure below is just for a reference.)
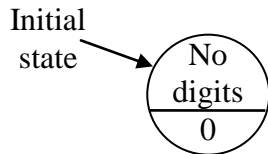

Constant logic 1

$\overline{S}$

$\overline{R}$

D

Clock

Q
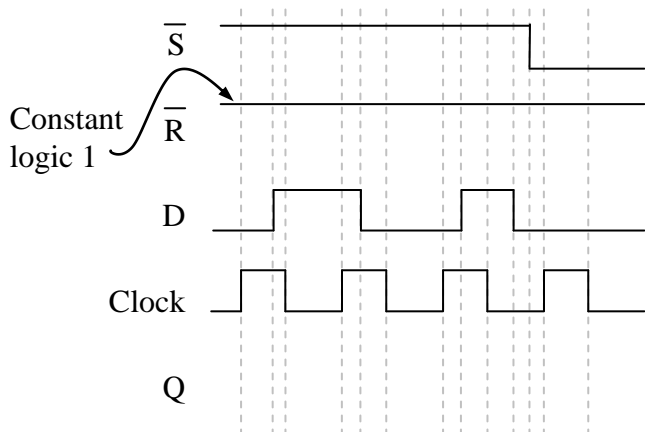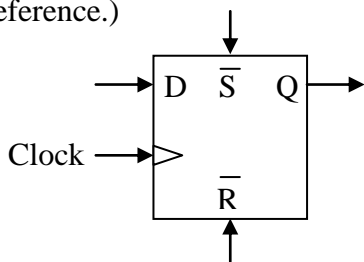
29. Make the state diagram that will output a '1' when the sequence '100' is detected in a serial stream of bits. For example, if the following binary stream is received:

    1 0 1 0 1 1 1 0 **1 0 0** 1 0 1 **1 0 0** 0 1 1 0 1 1 **1 0 0** 1 0

    then 1's will be output at these points. At all other times, the system will output zeros. Label the input D. (7 points)

30. Create the next state truth table and the output truth table for the state diagram to the right. The states have already been numbered. Use the variable names S_1 and S_0 to represent the most significant and least significant bits respectively of the binary number identifying the state. Label the output 'X'. (7 points)
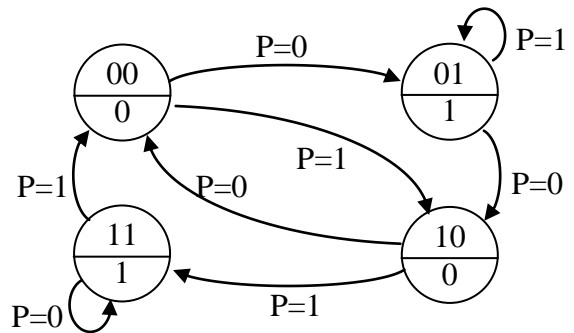
31. Derive the minimum SOP expression from the Karnaugh map below. (6 points)

AB \ CD	00	01	11	10
00	0	0	1	0
01	0	1	1	1
11	0	0	1	1
10	0	0	1	0

32. The three Boolean expressions below represent the ***next state bits (S_0' and S_1')*** and the ***output bit X*** based on the ***current state (S_0 and S_1)*** and the ***input A***. Draw the logic circuit for the state machine including the latches and output circuitry. ***Be sure to label the latch inputs and other signals.*** (7 points)

$$S_0' = \overline{A} \qquad\qquad S_1' = S_0 + S_1 \qquad\qquad X = \overline{S_1 \cdot S_0}$$