Points missed: _____ Student's Name: _____

Total score: _____ /100 points

East Tennessee State University
Department of Computer and Information Sciences
CSCI 2150 (Tarnoff) – Computer Organization
TEST 2 for Fall Semester, 2008

Read this before starting!

- The total possible score for this test is 100 points.
- This test is ***closed book and closed notes.***
- ***Please turn off all cell phones & pagers during the test.***
- **All** answers **must** be placed in space provided. Failure to do so may result in loss of points.
- **1 point** will be deducted per answer for missing or incorrect units when required. **No** assumptions will be made for hexadecimal versus decimal, so you should always include the base in your answer.
- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.
- ***Calculators are not allowed.*** Use the tables below for any conversions you may need. Leaving numeric equations is fine too.

Binary	Hex
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7

Binary	Hex
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Power of 2	Equals
2^3	8
2^4	16
2^5	32
2^6	64
2^7	128
2^8	256
2^9	512
2^{10}	1K
2^{20}	1M
2^{30}	1G

"Fine print"

Academic Misconduct:

Section 5.7 "Academic Misconduct" of the East Tennessee State University Faculty Handbook, June 1, 2001:

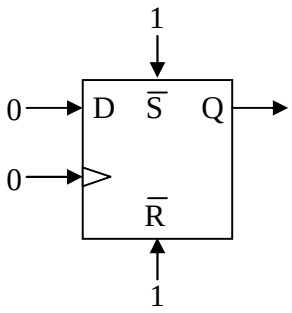
"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarism, the changing of falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of 'F' on the work in question, a grade of 'F' of the course, reprimand, probation, suspension, and expulsion. For a second academic offense the penalty is permanent expulsion."

Short answers – 2 points each unless otherwise noted

For the following ***three*** circuits, identify the value of the output Q from the following choices. Consider the D-latch a ***rising edge triggered latch***. (1 point each)

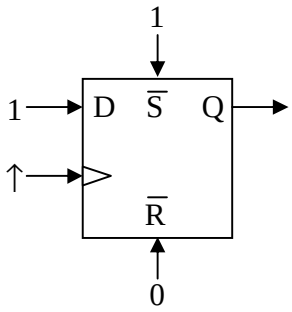
a.) 1 b.) 0 c.) Q_0 (stored value of Q) d.) undefined/illegal e.) can't tell

1.



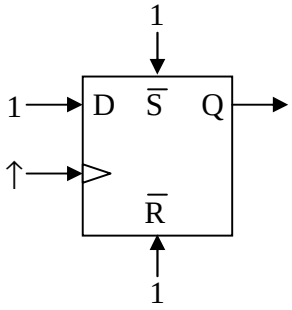
Answer: c
First, neither the R-bar or S-bar lines are 0. Therefore, we can look at D and the clock to see what Q might be. Since the D-latch is rising edge triggered, and the input the clock is a stable 0,i.e., it is not transitioning, then D has no effect on Q and Q is simply outputting the stored value of Q, i.e., Q_0.

2.



Answer: b
It doesn't matter what D and the clock are in this case since R-bar is set to 0. R-bar and S-bar override the clock and D. When R-bar equals zero, the output Q is reset to 0.

3.



Answer: a
Once again, neither the R-bar or S-bar lines are 0. Therefore, we can look at D and the clock to see what Q might be. This time, however, the clock is rising and therefore, the value at D is being stored to Q. Since D=1, then a 1 is being stored to Q.

4. A transparent active low D-latch copies data from the D input to the Q output:

a.) the instant the clock changes from a 1 to a 0
b.) the instant the clock changes from a 0 to a 1
c.) as long as the clock equals 0
d.) as long as the clock equals 1

Remember that a transparent latch sends D straight through to Q as long as the clock is at one level or the other. It acts much like a camera shutter remaining open as long as the user's finger remains on the button. An active-low transparent latch allows D to go straight through to Q ***as long as the clock equals zero***, i.e., the clock is low.

5. If you were to make an ***un-simplified*** Product-of-Sums expression directly from the truth table shown to the right, how many "sums" would it have? For example, the POS expression $(\overline{A}+B+C)\cdot(A+\overline{B}+\overline{C})\cdot(A+B+C)$ contains three sums.

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

a.) 1 b.) 2 c.) 3 d.) 4 e.) 5 f.) 6

Remember that a product-of-sums expression is derived from the ***ZEROS*** in the truth table. For each row where there is a zero, there will be a resulting sum. These sums will then all be ANDed together. Since the truth table to the right has 2 zeros, there will be two sums.

This was not part of the problem, but the POS expression for the truth table is $(A+\overline{B}+C)\cdot(\overline{A}+B+C)$. Notice the two sums.

6. True or false: The boolean expression $X=\overline{A}\cdot B\cdot C+\overline{A}\cdot B\cdot\overline{C}+A\cdot B$ is in proper Sum-of-Products format.

Nothing is wrong with this SOP expression. Basically what you're looking for when you examine whether a Boolean expression is in valid SOP form is whether or not it can be realized in the standard format of inputs going directly to AND gates (with possible inverted inputs) and all of the AND gates outputting to a single OR gate (no inverters between the ANDs and the ORs).

7. In the space below, write the product that represents the boolean expression for X in the truth table to the right.

A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

There is a single row with a one in it, specifically when A=0, B=0, and C=1. Therefore, the verbal way of describing this truth table is that X=1 when A=0 and B=0 and C=1, i.e., X=1 when not-A=1 and not-B=1 and C=1. This gives us the expression:

$$X=\overline{A}\cdot\overline{B}\cdot C$$

8. How many cells would a four-input (four-variable) Karnaugh Map have?

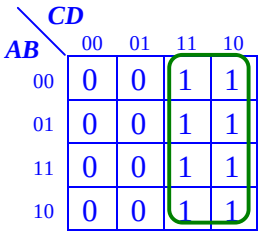
a.) 2 b.) 4 c.) 6 d.) 8 e.) 12 f.) 16 g.) 32

Since a Karnaugh map must have a cell for every pattern of 1's and 0's for all of the inputs, and since a 4-input circuit has $2^4 = 16$ possible combinations of 1's and 0's, then the answer is 16 cells.

9. In a four-variable Karnaugh map, how many input variables (A, B, C, and/or D) does a single product have if its corresponding rectangle of 1's contains 8 cells?

a.) 1 b.) 2 c.) 3 d.) Cannot be determined

The simplest way to answer this question is to create a 4-variable/input Karnaugh map that has a rectangle with eight 1's, then figure out what the product is. The number of inputs in the product will give us our answer.



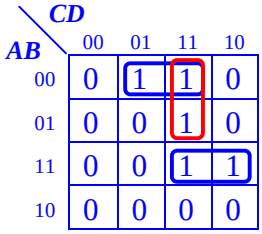
A	B	C	D	
0	0	1	1	C
0	0	1	0	
0	1	1	1	
0	1	1	0	
1	1	1	1	
1	1	1	0	
1	0	1	1	
1	0	1	0	

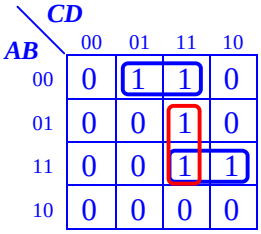
The rectangle has only one input, C, that remains constant. Therefore, the resulting product consists only of C. You'll find that regardless of how the 8-cell rectangle is arranged, the resulting product will always have 1 input.

Another way of doing this is to realize that one variable drops out every time the size of a rectangle is doubled. For an eight-cell rectangle, the rectangle doubled three times, once for 1 to 2 cells, once for 2 to 4 cells, then again for 4 to 8 cells. This means only 1 variable out of the 4 is left.

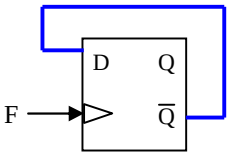
10. True or False: If done properly, there is exactly one possible arrangement for all of the rectangles of ones in a Karnaugh map.

All it takes is finding one case where this isn't true. The following is one of those cases.

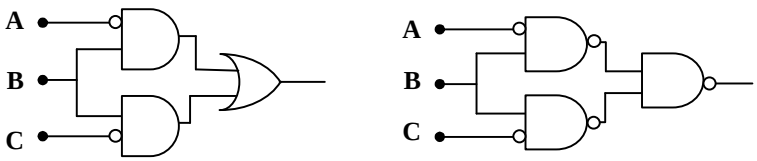




11. Make the connections to the latch in the figure to the right that makes a divide-by-two circuit, i.e., divides the frequency F in half at the output Q.

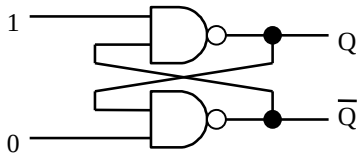


12. True or False: The two circuits below are equal.



TRUE: Remember that an OR gate is equivalent to a NAND gate with inverted inputs. Therefore, all of the gates of an SOP circuit can be replaced with NAND gates. (See section 6.7 NAND-NAND logic of the textbook.)

13. For the circuit to the right, what value does Q have? (2 points)

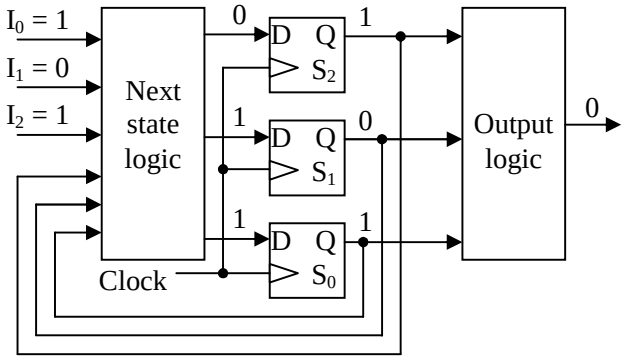


a.) 0 c.) Must know previous value for Q to answer.
b.) 1 d.) Illegal state. Should never have these inputs.

With this circuit, you must start by examining the NAND gate that has a zero at its input. In this case it is the lower NAND gate. A NAND gate with a 0 at any of its inputs MUST output a 1, i.e., the only way a NAND gate outputs a zero is if all of its inputs are 1.

This means that the input to the upper NAND gate is 1-1. Since all of the inputs of this NAND gate are 1, the output Q is 0.

The next six problems use the state machine circuit to the right. Assume that the states are numbered so that bit S_3 is the most significant bit and bit S_0 is the least significant bit.



14. What is the maximum number of states that this system can handle?

Since there are three latches, then the internal memory of this state machine can remember $2^3 = 8$ states: 000, 001, 010, 011, 100, 101, 110, and 111. Therefore, the answer is 8.

15. What is the current state of this system? Keep your answer in binary.

The current state is the value stored in the latches and found at the Q outputs. In the case of the diagram above, that is 1-0-1 with S_2 being the most significant bit.

16. If the clock were to pulse right now, what would the next state be? Keep your answer in binary.

The next state is the value present at the D inputs, i.e., the value that would be stored if we had a clock pulse occur. In the case of the diagram above, that is 0-1-1 with S_2 being the most significant bit.

S_2	S_1	S_0	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

17. The truth table to the right represents the output logic truth table for the above state machine. Circle the row that identifies the current output condition of the system, i.e., which row is represented by the ***current state*** of the logic in the diagram above without having any clock pulses occur?

The output is determined by the current state, i.e., 1-0-1. Therefore, the sixth row identifies the output, which fortunately equals 0 just like the figure.

18. If the clock were to pulse right now, what would the new output be? Use the truth table from the previous problem to answer the question.

a.) 0 b.) 1 c.) Not enough information given

The next state is 0-1-1. Looking at the truth table, we see that the output for the state 0-1-1 is 0.

19. How many rows would the next state logic truth table have for this circuit?

a.) $2^2 = 4$ b.) $2^3 = 8$ c.) $2^4 = 16$ d.) $2^5 = 32$ e.) $2^6 = 64$ f.) $2^7 = 128$

The next state logic is the logic to the right of the latches that is used to determine the next state of the system. In the case of this circuit, the next state logic truth table depends on the current state (derived from S_2, S_1, and S_0) and the system's inputs (I_2, I_1, and I_0). This gives us 6 inputs. Since there are $2^6 = 64$ combinations of 1's and 0's for 6 inputs, the answer is e. (Counting the arrows into the block labeled "Next state logic" would have also shown that there are 6 inputs to this logic.)

20. True or False: Re-numbering the states of a state machine has no effect on the "next state" logic for the digital hardware implementation.

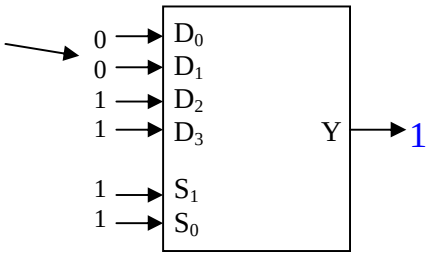
The numbering of the states directly affects the next state truth table, and therefore changes the logic that is derived from it. Therefore, the answer is **False**.

21. How many latches will a state machine with 64 states require?

a.) 3 b.) 4 c.) 5 d.) 6 e.) 7 f.) 8 g.) 9

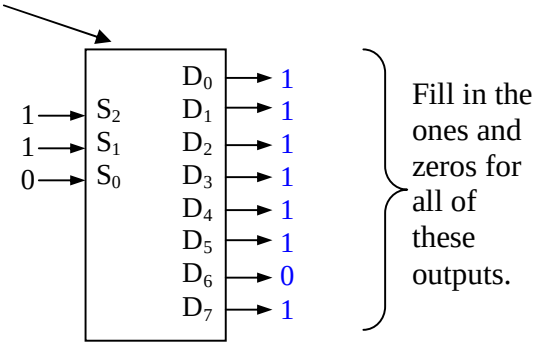
With 64 states, they would be numbered 0, 1, 2, 3, … , 62, and 63. Since $63_{10} = 111111_2$, a binary value with 6 bits, we will need 6 bits to represent the state. **Therefore, the answer is d.** Another way of looking at it is to see how many states it is possible to represent with n bits, and to figure out what value of 2^n is greater than or equal to 24 different values. $2^4 = 16$ which is not enough, $2^5=32$ which is still not enough, but $2^6=64$ which is exactly what is needed. Therefore, 6 bits will do the trick.

22. For the multiplexer/selector shown to the right, what is the output Y equal to?



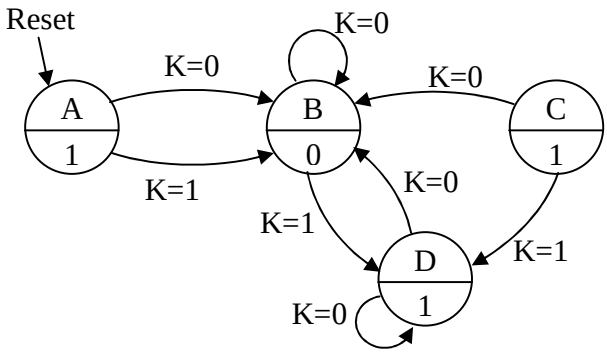
The input that is being routed to the output is "selected" by the selector inputs S_1 and S_0 with S_1 being the most significant bit. The digital value of these two bits is 11_2 which equals a decimal 3. Therefore, the input D_3 is going to be routed to the output Y making Y have an output of 1.

23. For the ***active-low*** output decoder shown to the right, fill in the values for all of the outputs D_0 through D_7. Assume S_2 is most significant bit of the inputs.



Remember that the bits S_2, S_1, and S_0 make up a digital selector with S_2 being the most significant bit. The digital value of these three bits is 110_2 which when converted to decimal gives us 6. That means that output D_6 is the selected output. Since it's active low, there will be a zero output on D_6 and 1's everywhere else.

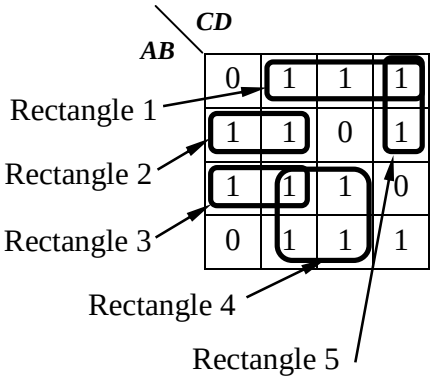
24. Identify the 2 errors in the state diagram to the right. The circuit is to have a single binary input K. Do not bother to correct the errors. (2 points for each error identified correctly)



There are two things to look for when "troubleshooting" a state diagram. First, be sure that there is a way to get to every state. This means that every state must have at least one transition/edge with an arrow pointing into the state. (The Reset arrow counts as an arrow.) State C has no arrow going into it.

Second, make sure that there exists a transition/edge pointing out of every state for every possible input combination. In our case, that means that there must be an arrow coming out of every state for K=1 and for K=0. This is not the case for state D. State D has two arrows, but they are both for K=0. This is not allowed.

25. For the Karnaugh map to the right, identify three ***mistakes*** with how the rectangles have been made. Note that not all of the problems may be with a specific rectangle, but if there is a problem with a rectangle, be sure to identify it using the names given. (2 points each)



Mistake 1: Rectangle one encloses 3 cells. Three is not a power of 2.

Mistake 2: Rectangles 2 and 3 should be combined as neither one is as large as it could be, but together they make a legal, 4-cell rectangle.

Mistake 3: There is a 1 left uncovered in the bottom right cell of the Karnaugh map.

Medium answers – 4 points each

26. Complete the truth table to the right with the values for the sum-of-products expression $A + B \cdot \overline{C}$.

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Remember that each product generates a 1 when all of its inputs are one, e.g., $1 \cdot 1 \cdot 1 = 1$. This means that if we can figure out where each product equals 1, we know where the 1's are in the truth table. The remaining positions are filled with zeros.

The first product, A, equals one when A=1. Therefore, any rows where A=1 should be set to 1. This includes the bottom four rows.

The second product, $B \cdot \overline{C}$, equals 1 when B=1 and when C=0. This happens in the third and seventh rows of the truth table. The seventh row is already a 1 from the product A.

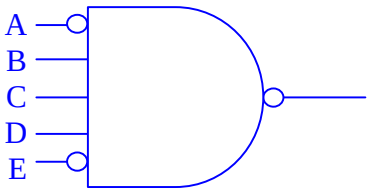
This gives us the pattern of 1's and 0's you see filled in above.

27. In the Karnaugh map to the right, draw the best pattern of rectangles you can. ***Do not derive the SOP expression.***

AB \ CD	00	01	11	10
00	0	0	0	1
01	X	X	X	X
11	0	0	1	1
10	1	1	1	1

Remember to only include X's in rectangles if they make the rectangle bigger. Do not include an X if it adds an additional rectangle. Note that the 2×2 rectangle (the green one) could have been moved up to include the two X's above it and not the lower two ones. This can be done because the rectangle that covers the bottom row already takes care of the ones. This would have given a slightly different SOP expression.

28. In the space to the right, draw the decoding logic circuit with an active-low output that identifies when A = 0, B = 1, C = 1, D = 1, and E = 0.

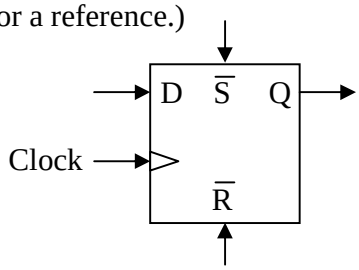


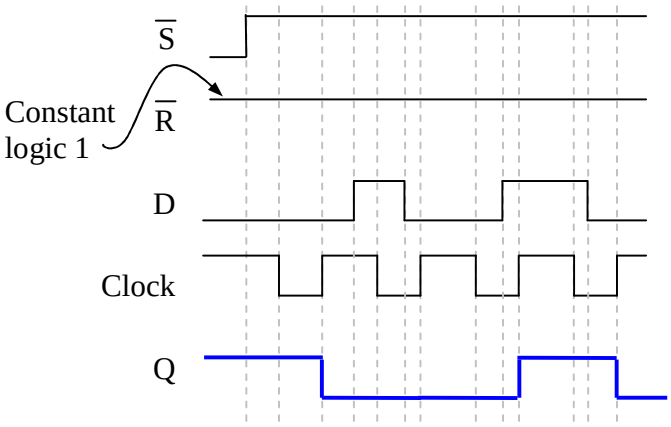
29. Create a Karnaugh map from the truth table below. ***Do not worry about making the rectangles.***

A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

AB \ C	0	1
00	0	1
01	0	1
11	1	1
10	0	0

30. Show the *D* latch output waveform *Q* based on the inputs *D*, $\overline{S}$, $\overline{R}$, and clock indicated in the graph to the right. Assume the latch captures on the rising edge. (The figure below is just for a reference.)

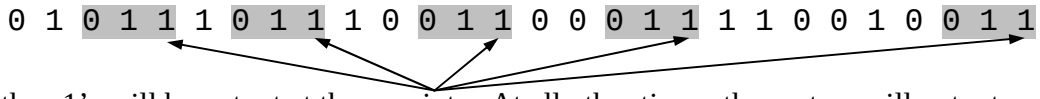




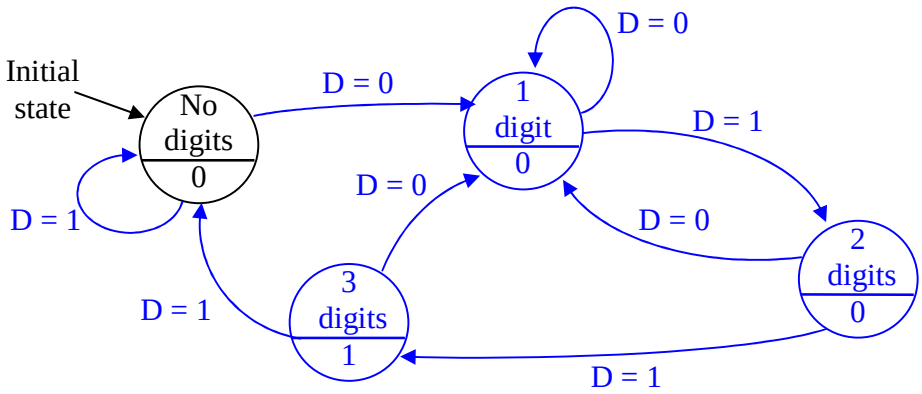
Note that since S-bar is 0 at the very beginning of the timing diagram, Q should start as a 1, i.e., the set condition. Once both S-bar and R-bar are both high, then the rising edge of the clock will copy D to Q. The first time this happens, D is equal to zero, so Q is set to zero The rising edge of the second clock pulse stores a 0 from D to Q, so it looks like nothing changes. The third clock pulse stores a 1 from D to Q. Finally, the fourth clock pulse stores a 0 to Q from D.

Longer answers – Points vary per problem

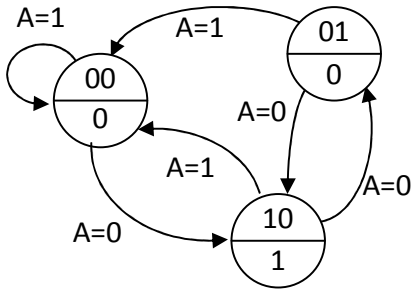
31. Make the state diagram that will output a '1' when the sequence '011' is detected in a serial stream of bits. For example, if the following binary stream is received:



then 1's will be output at these points. At all other times, the system will output zeros. ***Label the input D.*** (7 points)



32. Create the next state truth table and the output truth table for the state diagram to the right. The states have already been numbered. Use the variable names S_1 and S_0 to represent the most significant and least significant bits respectively of the binary number identifying the state. Label the output 'X'. (7 points)



Remember that the next state truth table represents a one-to-one mapping of each of the transitions (arrows) from one state to the next state. This means it depends on the current state defined by S_0 and S_1 and the input, A. The output truth table is a one-to-one mapping of the current state to the output value contained in the circle, i.e., the output is the value below the line while the value of S_1 and S_0 is shown above the line.

Now this problem has a "trick". There are only three states which means that the four possible value for S_1 and S_0 of "11" is not defined. Therefore any row in the truth table with S_1=1 and S=1 will be a "don't care" represented with an 'X'.

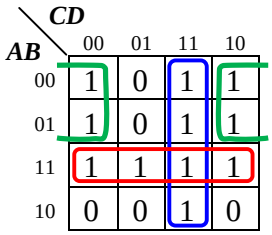
Output T.T.

S_1	S_0	X
0	0	0
0	1	0
1	0	1
1	1	X

Next State T.T.

S_1	S_0	P	S_1'	S_0'
0	0	0	1	0
0	0	1	0	0
0	1	0	1	0
0	1	1	0	0
1	0	0	0	1
1	0	1	0	0
1	1	0	X	X
1	1	1	X	X

33. Derive the minimum SOP expression from the Karnaugh map below. (6 points)



AB \ CD	00	01	11	10
00	1	0	1	1
01	1	0	1	1
11	1	1	1	1
10	0	0	1	0

Red rectangle

A	B	C	D
1	1	0	0
1	1	0	1
1	1	1	1
1	1	1	0

C and D drop out. Since A=1 and B=1, neither needs to be inverted in the product.

$A \cdot B$

Blue rectangle

A	B	C	D
0	0	1	1
0	1	1	1
1	1	1	1
1	0	1	1

A and B drop out. Since C=1 and D=1, neither needs to be inverted in the product.

$C \cdot D$

Green rectangle

A	B	C	D
0	0	0	0
0	1	0	0
0	0	1	0
0	1	1	0

B and C drop out. Since both A=0 and D=0, they are inverted in the product.

$\overline{A} \cdot \overline{D}$

The final answer is:

$A \cdot B + C \cdot D + \overline{A} \cdot \overline{D}$

34. The three Boolean expressions below represent the ***next state bits (S_0' and S_1')*** and the ***output bit X*** based on the ***current state (S_0 and S_1)*** and the ***input A***. Draw the logic circuit for the state machine including the latches and output circuitry. ***Be sure to label the latch inputs and other signals.*** (7 points)

$S_0' = \overline{S_1}$ $\quad S_1' = A \cdot S_0$ $\quad X = S_0$