

Points missed: \_\_\_\_\_ Student's Name: \_\_\_\_\_

Total score: \_\_\_\_\_/100 points

East Tennessee State University  
Department of Computer and Information Sciences  
CSCI 2150 (Tarnoff) – Computer Organization  
TEST 2 for Spring Semester, 2004

## Section 002

**Read this before starting!**

- The total possible score for this test is 100 points.
- This test is closed book and closed notes.
- **All** answers **must** be placed in space provided. Failure to do so may result in loss of points.
- **1 point** will be deducted per answer for missing or incorrect units when required. **No** assumptions will be made for hexadecimal versus decimal, so you should always include the base in your answer.
- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.
- **Calculators are not allowed.** Use the tables below for any conversions you may need. Leaving numeric equations is fine too.

Binary	Hex
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7

Binary	Hex
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Power of 2	Equals
$2^3$	8
$2^4$	16
$2^5$	32
$2^6$	64
$2^7$	128
$2^8$	256
$2^9$	512
$2^{10}$	1K
$2^{20}$	1M
$2^{30}$	1G

“Fine print”

Academic Misconduct:

Section 5.7 "Academic Misconduct" of the East Tennessee State University Faculty Handbook, June 1, 2001:

"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarism, the changing of falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of 'F' on the work in question, a grade of 'F' of the course, reprimand, probation, suspension, and expulsion. For a second academic offense the penalty is permanent expulsion."

1. How many cells does a 3 input variable Karnaugh map have? (2 points) 8

There must be a cell for each combination of one's and zero's of the input variables, and since 3 input variables have  $2^3 = 8$  combinations of one's and zero's, then the K-map must have 8 cells.

2. What is the largest number of input variables a Karnaugh map can handle and still remain 2-dimensional? (2 points) 4

The answer is 4. Going to 5 variables would force either the columns or the rows to represent 3 variables, which is 8 combinations of 1's and 0's. It is impossible to label 8 rows with three binary variables so that only one binary variable changes between adjacent rows

3. In a 3-variable Karnaugh map, how many input variables, A, B, or C, does a product have if its rectangle of 1's contains 2 cells? Your answer should be 0, 1, 2, or 3. (2 points) 2

Remember that each time the size of a rectangle is doubled (e.g., 1 cell doubled to 2 cells, 2 cells doubled to 4 cells, and so on) a single input variable drops out. In addition, a rectangle of size 1 uses all of the input variables. Therefore, since a rectangle of 2 cells has doubled exactly once over the size of a single cell rectangle, there is 1 variable that has dropped out. **Therefore, a product from a rectangle of two cells in a 3-variable K-map has 2 variables.** (You could also show this by creating an example.)

4. Create a Karnaugh map from the truth table below. Do not worry about making the rectangles. (5 points)

A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

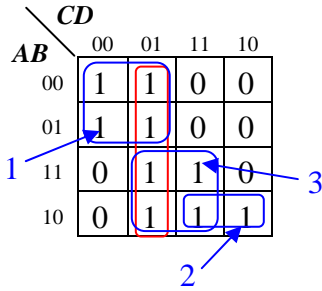
		C	
		0	1
AB	00	0	1
	01	1	0
	11	1	0
	10	0	1

5. In the Karnaugh map to the right, draw the best pattern of rectangles you can. **Do not derive the SOP expression.** (4 points)

Note that if you didn't include the lower two cells with X's in the right rectangle, your rectangle would have been too small and would have created a product with more variables. If you added a rectangle to include the other two X's, then you added a product, and therefore made a more complex SOP expression.

		CD			
		00	01	11	10
AB	00	1	1	0	1
	01	0	0	0	1
	11	0	0	X	X
	10	0	0	X	X

6. Derive the minimum SOP expression from the Karnaugh map below. (6 points)



Note that the red rectangle is a duplicate of the others and should be removed.

Rectangle 1

A	B	C	D
0	0	0	0
0	1	0	0
0	0	0	1
0	1	0	1

B and D drop out and A and C are inverted.

$$\bar{A} \cdot \bar{C}$$

Rectangle 2

A	B	C	D
1	0	1	1
1	0	1	0

D drops out, A and C are not inverted, but B is.

$$A \cdot \bar{B} \cdot C$$

Rectangle 3

A	B	C	D
1	1	0	1
1	1	1	1
1	0	0	1
1	0	1	1

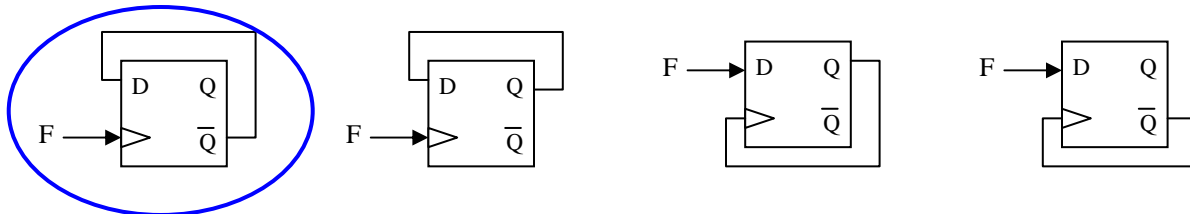
B and C drop out and A and D are not inverted.

$$A \cdot D$$

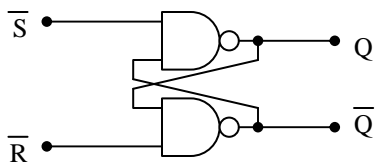
The final answer is:

$$\bar{A} \cdot \bar{C} + A \cdot D + A \cdot \bar{B} \cdot C$$

7. Place a circle around the circuit below that can be used to divide the *frequency* of the input F by 2. (3 points)

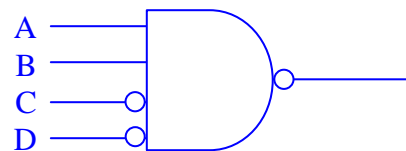


8. Fill out the truth table to the right for all possible combinations of inputs for the circuit below. (5 points)

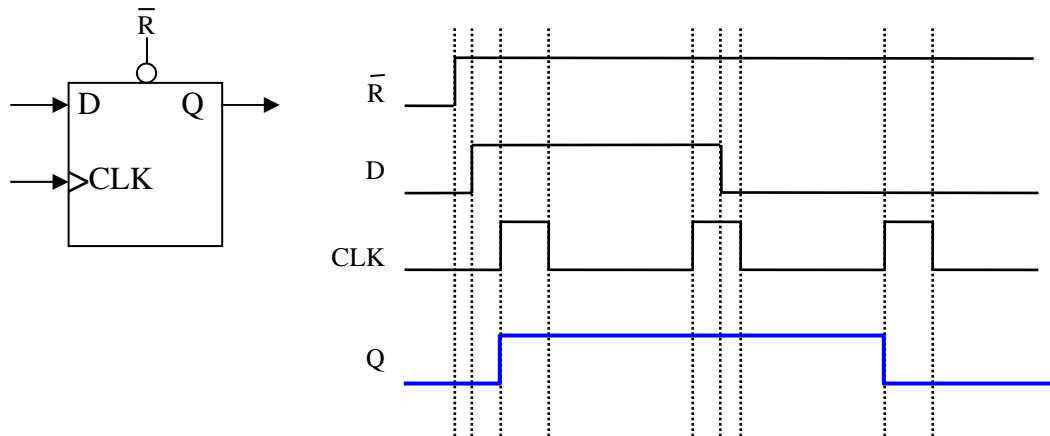


$\bar{S}$	$\bar{R}$	Q	$\bar{Q}$
0	0	Illegal	
0	1	1	0
1	0	0	1
1	1	$Q_0$	$\bar{Q}_0$

9. In the space to the right, draw the *decoding logic circuit* with an *active-low output* for the inputs A = 1, B = 1, C = 0, and D = 0. (5 points)



10. Show the D flip-flop output waveform Q based on the inputs D and CLK indicated in the figure below. Assume the flip-flop captures on the rising edge. (6 points)

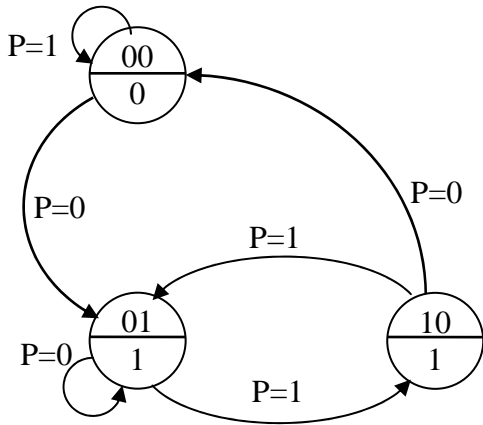


It's important to note that  $\bar{R}$  going low before the first clock pulse forces Q to 0.

11. How many latches or flip-flops are needed to realize a state machine with 16 states? (3 points)

Sixteen states would be numbered 0, 1, 2, 3, ..., 14, and 15. Since  $15_{10}$  equals  $1111_2$ , then four bits are needed to represent each state of the state machine. Therefore, **4 latches would be required.**

12. Create the next state truth table and the output truth table for the state diagram below. Use the variable names  $S_1$  and  $S_0$  to represent the most significant and least significant bits respectively of the binary number identifying the state. (8 points)



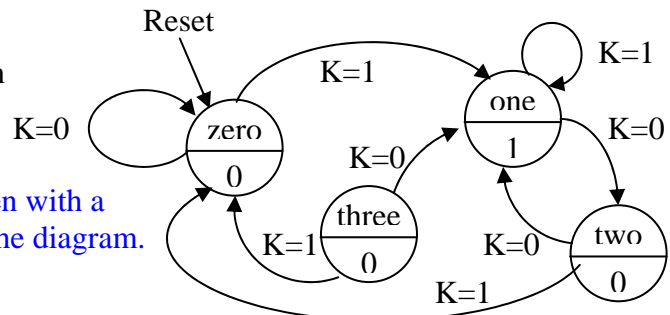
Next State T.T.

$S_1$	$S_0$	P	$S_1'$	$S_0'$
0	0	0	0	1
0	0	1	0	0
0	1	0	0	1
0	1	1	1	0
1	0	0	0	0
1	0	1	0	1
1	1	0	X	X
1	1	1	X	X

Output T.T.

$S_1$	$S_0$	X
0	0	0
0	1	1
1	0	1
1	1	X

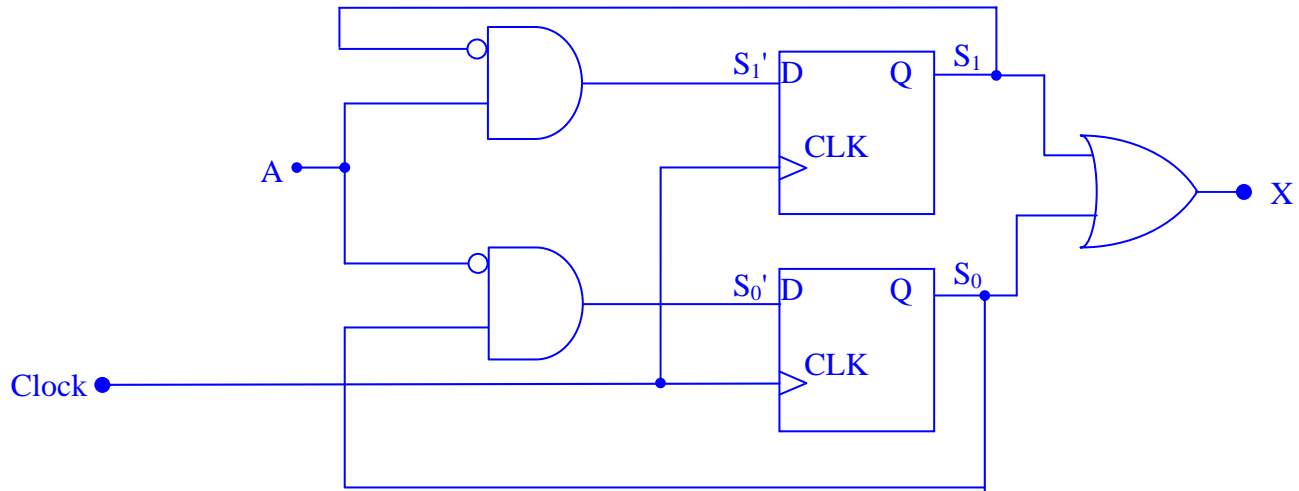
13. Identify the error in the state diagram shown to the right. (3 points)



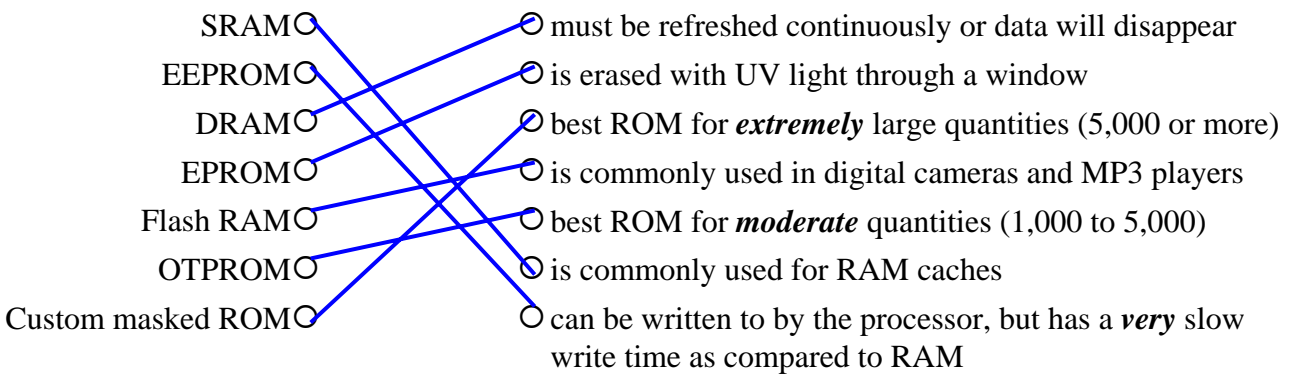
There is no way to get to state three, not even with a reset. Therefore, it must be removed from the diagram.

14. The three Boolean expressions below represent the *next state bits* ( $S_0'$  and  $S_1'$ ) and the *output bit*  $X$  based on the *current state* ( $S_0$  and  $S_1$ ) and the *input*  $A$ . Draw the logic circuit for the state machine including the flip-flops and output circuitry. Be sure to label flip-flop inputs and other signals.

(8 points)  $S_0' = \bar{A} \cdot S_0$                        $S_1' = \bar{S}_1 \cdot A$                        $X = S_0 + S_1$



15. Draw a line between the memory type on the left and its most appropriate characteristic on the right. (10 points)



Note that the points taken off correspond to the following: 2 wrong: -1; 3 wrong: -3; 4 wrong: -5; 5 wrong: -7; 6 wrong: -9; and 7 wrong: -10.

16. How many D latches or flip-flops are contained in a RAM memory that has 20 address lines and 8 data lines? (Don't do the calculation; only write the equation with the correct values.) (3 points)

$$2^{20} * 8 = 8K$$

17. Which of the following settings of the memory bus signals  $\bar{R}$  and  $\bar{W}$  occurs when the processor is storing data to memory? (2 points)

- a.)  $\bar{R} = 0, \bar{W} = 0$       b.)  $\bar{R} = 0, \bar{W} = 1$       **c.)  $\bar{R} = 1, \bar{W} = 0$**       d.)  $\bar{R} = 1, \bar{W} = 1$       e.) None



Note that a vertical division can be made between the binary values that remain constant ( $A_{13}$  through  $A_{15}$ ) and the values that change from all zeros to all ones ( $A_0$  through  $A_{12}$ ). Therefore, this is a valid memory space for a single memory and the answer is **TRUE**.

23. Using logic gates, design an active low chip select for a RAM placed in a 1 Meg memory space with a low address of  $18000_{16}$  and a high address of  $1BFFF_{16}$ . *Label all address lines used for chip select.* (7 points)

Begin by converting  $18000_{16}$  and  $1BFFF_{16}$  to binary. *Remember that a processor with a 1 Meg memory space requires 20 address lines ( $1 \text{ Meg} = 2^{20}$ ), so be sure to convert to binary values with 20 digits.*

$$18000_{16} = 0001\ 1000\ 0000\ 0000\ 0000_2$$

$$1BFFF_{16} = 0001\ 1011\ 1111\ 1111\ 1111_2$$

	$A_{19}$	$A_{18}$	$A_{17}$	$A_{16}$	$A_{15}$	$A_{14}$	$A_{13}$	$A_{12}$	$A_{11}$	...	$A_5$	$A_4$	$A_3$	$A_2$	$A_1$	$A_0$
Low address =	0	0	0	1	1	0	0	0	0	...	0	0	0	0	0	0
High address =	0	0	0	1	1	0	1	1	1	...	1	1	1	1	1	1

Note that the dividing line between the bits that remain constant and the bits that change from all ones to all zeros is between address lines  $A_{13}$  and  $A_{14}$ . Therefore,  $A_{14}$  through  $A_{19}$  will be the inputs to the chip select circuitry.

The chip select is always made from a NAND gate with the inputs that are meant to be zeros going through inverters. The result is shown in the answer below.

