

Points missed: _____ Student's Name: _____

Total score: _____/100 points

East Tennessee State University
Department of Computer and Information Sciences
CSCI 2150 (Tarnoff) – Computer Organization
TEST 2 for Spring Semester, 2007

Read this before starting!

- The total possible score for this test is 100 points.
- This test is *closed book and closed notes*.
- *Please turn off all cell phones & pagers during the test.*
- **All** answers **must** be placed in space provided. Failure to do so may result in loss of points.
- **1 point** will be deducted per answer for missing or incorrect units when required. **No** assumptions will be made for hexadecimal versus decimal, so you should always include the base in your answer.
- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.
- **Calculators are not allowed.** Use the tables below for any conversions you may need. Leaving numeric equations is fine too.

Binary	Hex
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7

Binary	Hex
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Power of 2	Equals
2^3	8
2^4	16
2^5	32
2^6	64
2^7	128
2^8	256
2^9	512
2^{10}	1K
2^{20}	1M
2^{30}	1G

“Fine print”

Academic Misconduct:

Section 5.7 "Academic Misconduct" of the East Tennessee State University Faculty Handbook, June 1, 2001:

"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarizing, the changing or falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of 'F' on the work in question, a grade of 'F' of the course, reprimand, probation, suspension, and expulsion. For a second academic offense the penalty is permanent expulsion."

Short answers – 2 points each unless otherwise noted

For the following **two** circuits, identify the value of the output Q from the following choices. Consider the D-latch a **rising edge triggered latch**.

- a.) 1 b.) 0 c.) Q_0 (stored value of Q) d.) undefined/illegal e.) can't tell

1. Answer: C

Since this is a rising edge triggered latch, a falling edge has no effect, and therefore, Q_0 remains unchanged.

2. Answer: A

With both S^{\wedge} and R^{\wedge} high, the rising clock copies $D=1$ to Q.

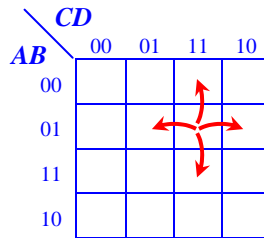
3. True or **False**: The expression $(A + \bar{B} + C) \cdot \overline{(B + A)}$ is in proper Product-of-Sums format.
 False: The inverted output of the sum $B + A$ puts an inverter between the output of one of the OR gates and the input of the final AND gate. In a POS circuit, all inverters must be at the OR inputs.

4. How many cells would a two-input Karnaugh Map have?
 There are $2^2 = 4$ possible combinations of 1's and 0's for two inputs. Therefore, since the Karnaugh map must have one cell for each combination, there are 4 cells.

- a.) 2 **(b.) 4** c.) 6 d.) 8 e.) 12 f.) 16 g.) 32

5. What is the largest number of input variables a Karnaugh map can handle and still remain two-dimensional?

Remember that the purpose of a Karnaugh map is to rearrange the truth table so that adjacent cells can be combined allowing for a term to drop out. In other words, the key to the effectiveness of Karnaugh maps is that each cell represents the output for a specific pattern of ones and zeros at the input, and that to move to an adjacent cell, exactly one of those inputs can change, the rest must remain the same. Take for instance the 16 cell (4-input) Karnaugh map. The cell in the third column of the second row represents the condition where $A=0, B=1, C=1,$ and $D=1$. Moving to the cell immediately to the left will change only C; moving right will change D; moving up changes B; and moving down changes A. Therefore, there is an adjacent cell that represents a change in any of the four input variables.



Since a square only has 4 sides, it can only represent 4 single-bit changes in the inputs. Therefore, 4 is the maximum.

- a.) 2 b.) 3 **(c.) 4** d.) 5 e.) 6 f.) 7 g.) 8

6. In a 3-variable Karnaugh map, how many input variables (A, B, and/or C) does a product have if its corresponding rectangle of 1's contains 2 cells?

The simplest way to answer this question is to create a 3-variable/input Karnaugh map that has a rectangle with two 1's, then figure out what the product is. The number of inputs in the product will give us our answer.

	C	0	1
AB	00	0	0
	01	0	0
	11	1	1
	10	0	0

A	B	C
1	1	0
1	1	1
$A \cdot B$		

The resulting product has two inputs. You'll find that regardless of how the 2 cell rectangle is arranged, the resulting product will always have 2 inputs.

- a.) 1 **b.) 2** c.) 3 d.) Cannot be determined

7. If $D = 0$ and the clock equals 1 on an active high D latch, the output Q is equal to

When the clock on a transparent latch is active, the value at D is passed straight through to the output Q. The clock on an active high transparent is active when equal to 1. Therefore, in this situation the 0 at D is passed through to Q.

- a.) 1 **b.) 0** c.) Cannot be determined

8. **True** or False: A D latch with only two inputs D and CLK has no undefined/illegal states.

True: When it comes to latches, the only illegal state is when both the \bar{S} and \bar{R} inputs are equal to zero at the same time. Since this latch does not have these inputs, there are no illegal states.

9. An active low signal is idle/inactive when its value is

- a.) 1** b.) 0 c.) The term active low is not defined by the binary values 0 or 1

10. Which of the following expressions produces the truth table to the right?

- a.) $A \cdot \bar{B} + C$** b.) $A + C$ c.) $A \cdot B + C$
 d.) $B + C$ e.) $A + \bar{B} \cdot C$ f.) None of the above

A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

The easiest way I know to do this is to simply put together the truth table for each of the options a through e to see if any of them match. For example, $A \cdot \bar{B} + C$ is equal to 1 when $A \cdot \bar{B}$ equals 1 ($A=1$ and $B=0$) or when C equals 1. This gives us a truth table with a 1 in the following rows:

- $A=1, B=0, C=0$ $A=1, B=0, C=1$
 $A=0, B=0, C=1$ $A=0, B=1, C=1$ $A=1, B=0, C=1$ $A=1, B=1, C=1$

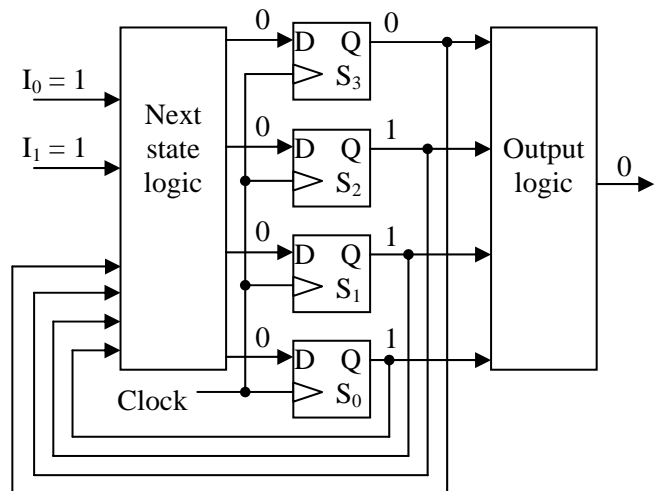
The first two are for $A=1$ and $B=0$ while the last four represent the times when $C=1$. All other rows will have zeros.

If we do this for all of the options a through e, we get the following truth tables. Column a equals 1 only when A=1 and B=0 or when C=1. Column b equals 1 when A=1 or when C=1. Column c equals 1 only when A=1 and B=1 or when C=1. Column d equals 1 when B=1 or when C=1. Column e equals 1 when A=1 or when B=0 and C=1. The only column that matches the original truth table exactly is column a. Therefore, the answer is a.

A	B	C	a	b	c	d	e
0	0	0	0	0	0	0	0
0	0	1	1	1	1	1	1
0	1	0	0	0	0	1	0
0	1	1	1	1	1	1	0
1	0	0	1	1	0	0	1
1	0	1	1	1	1	1	1
1	1	0	0	1	1	1	1
1	1	1	1	1	1	1	1

Column a is the only column that matches the original truth table. Therefore, the answer is a.

The next six problems use the state machine circuit to the right. Assume that the states are numbered so that bit S_3 is the most significant bit and bit S_0 is the least significant bit.



11. What is the maximum number of states that this system can handle?

Since there are four latches, then the internal memory of this state machine can remember $2^4 = 16$ states: 0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100, 1101, 1110, and 1111. Therefore, the answer is 16.

12. What is the current state of this system? Keep your answer in binary.

The current state is the value stored in the four latches and found at the Q outputs. In the case of the diagram above, that is 0111 with S_3 being used as the most significant bit.

13. If the clock were to pulse right now, what would the next state be? Keep your answer in binary.

The next state is the value present at the D inputs, i.e., the value that would be stored if we had a clock pulse occur. In the case of the diagram above, that is 0000 with S_3 being the most significant bit.

14. The truth table to the right represents the output logic truth table for the above state machine. Circle the row that identifies the current output condition of the system, i.e., which row is represented by the state of the logic in the diagram above?

S_3	S_2	S_1	S_0	X
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

The output is determined by the current state, i.e., 0111. Therefore, the seventh row identifies the output, which matches the 0 output from the figure.

15. If the clock were to pulse right now, what would the new output be? Use the truth table from the previous problem to answer the question.

a.) 0 b.) 1 c.) Not enough information given

Since the next state is 0000, we go to the row in the truth table for 0000. This shows us that the output for the next state is 0.

16. How many rows would the next state logic truth table have for this circuit?

a.) $2^2 = 4$ b.) $2^3 = 8$ c.) $2^4 = 16$ d.) $2^5 = 32$ e.) $2^6 = 64$

Remember that the next state logic truth table depends on the current state (derived from $S_3, S_2, S_1,$ and S_0) and the current input (I_1 and I_0). This gives us 6 inputs. Since there are $2^6 = 64$ combinations of 1's and 0's for 6 inputs, the answer is e.

17. True or False: Renumbering the states of a state machine has no effect on the "next state" logic for the digital hardware implementation.

The numbering of the states directly affects the next state truth table, and therefore changes the logic that is derived from it. Therefore, the answer is **False**.

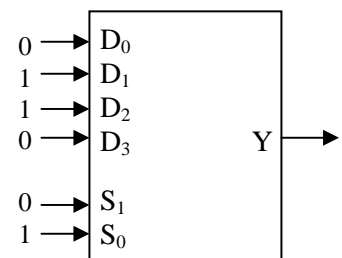
18. How many latches will a state machine with states numbered from 0 to 63 require?

a.) 3 b.) 4 c.) 5 d.) 6 e.) 7 f.) 8 g.) 9

With states numbered 0, 1, 2, 3, ..., and 63, there will be 64 states. Since $63_{10} = 111111_2$, we will need 6 bits to represent the state. **Therefore, the answer is d.** Another way of looking at it is to see how many states it is possible to represent with n bits, and to figure out what value of 2^n is greater than or equal to 64 different values. $2^4 = 16$ which is not enough, $2^5 = 32$ is still not enough, but $2^6 = 64$ is exactly enough. Therefore, 6 bits will do the trick.

19. For the multiplexer/selector shown to the right, what is the output Y?

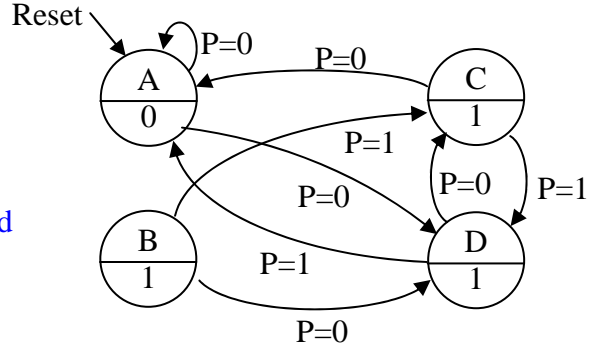
Remember that a multiplexer is like a digitally controlled channel changer using the inputs S_1 and S_0 , to select either $D_0, D_1, D_2,$ or D_3 to be output to Y. The way it works is that the decimal equivalent of the bits at the inputs S_1 and S_0 identify the subscript of the D input being routed to Y. Since S_1 and S_0 equal 0 and 1 respectively, and since $01_2 = 1_{10}$, then D_1 is routed to Y. Since D_1 equals 1, then the output at Y equals 1.



20. If a group of four rows or columns in a Karnaugh map is identified with two variables, it is numbered 00, 01, 11, 10 instead of 00, 01, 10, 11. Why?

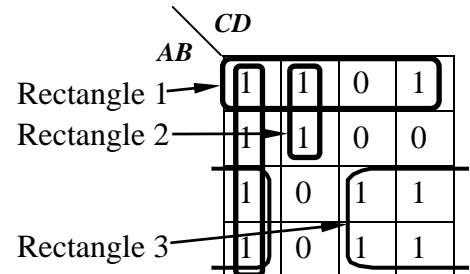
Because any horizontal or vertical movement between adjacent cells can only have 1 input variable change. Numbering 00, 01, 10, 11 has two variables changing when going from 01 to 10 and when wrapping around the table from 00 to 11. 00, 01, 11, 10 does not have this problem.

21. Identify the two errors in the state diagram to the right. The circuit is to have a single binary input B. Do not bother to correct the errors. (2 points for each error identified correctly)



1. State A has two transitions coming out of it labeled P=0. One of them needs to be changed to represent the P=1 state.
2. There is no way to get to state B. Therefore, it is an unneeded state.

22. For the Karnaugh map to the right, identify the problems with each of the three rectangles shown. (2 points each)



Rectangle 1: This rectangle contains a 0.

Rectangle 2: This rectangle could be made larger by doubling it toward the left to include the four ones in the upper left corner/quadrant.

Rectangle 3: This rectangle encloses a non-power of 2 number of cells, specifically 6.

Medium answers – 4 points each

23. Complete the truth table to the right with the values for the following sum-of-products expression:

$$\overline{A} \cdot \overline{B} + B \cdot C + A \cdot \overline{C}$$

Remember that each product generates a 1 when all of its inputs are one, e.g., $1 \cdot 1 \cdot 1 = 1$. This means that if we can figure out where each product equals 1, we know where the 1's are in the truth table. The remaining positions are filled with zeros.

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

$(\overline{A} \cdot \overline{B}) = 1$ when $A=0, B=0,$ and $C=0$ or 1

$(B \cdot C) = 1$ when $B=1, C=1,$ and $A=0$ or 1

$(A \cdot \overline{C}) = 1$ when $A=1, C=0,$ and $B=0$ or 1

24. In the Karnaugh map to the right, draw the best pattern of rectangles you can. **Do not derive the SOP expression.**

Remember to only include X's in rectangles if they make the rectangle bigger. Do not include an X if it adds an additional rectangle. There were actually two answers for this problem, both of which produced an optimal result.

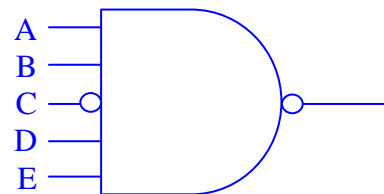
	CD			
AB	00	01	11	10
00	1	1	1	1
01	1	X	0	0
11	1	0	X	1
10	1	0	1	1

	CD			
AB	00	01	11	10
00	1	1	1	1
01	1	X	0	0
11	1	0	X	1
10	1	0	1	1

	CD			
AB	00	01	11	10
00	1	1	1	1
01	1	X	0	0
11	1	0	X	1
10	1	0	1	1

25. In the space to the right, draw the decoding logic circuit with an active-low output that identifies when $A = 1, B = 1, C = 0, D = 1,$ and $E = 1.$

An active-low decoder is meant to have a zero output for exactly one pattern of 1's and 0's at its inputs. This is done with a NAND gate where the inputs that are supposed to be 1 go straight into the inputs while the inputs that are supposed to be 0 pass through an inverter first.

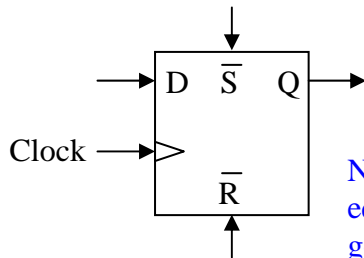


26. Create a Karnaugh map from the truth table below. **Do not worry about making the rectangles.**

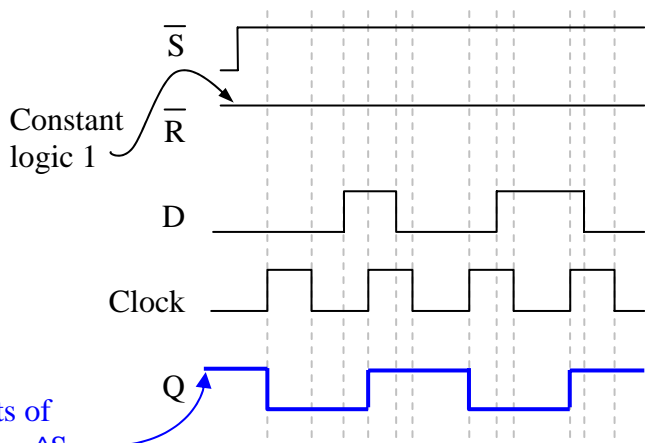
A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

	C	
AB	0	1
00	1	1
01	0	1
11	1	1
10	1	0

27. Show the D latch output waveform Q based on the inputs $D, \bar{S}, \bar{R},$ and clock indicated in the graph to the right. Assume the latch captures on the rising edge. (The figure below is just for a reference.)



Note that Q starts of equal to 1 because $\wedge S$ goes low.

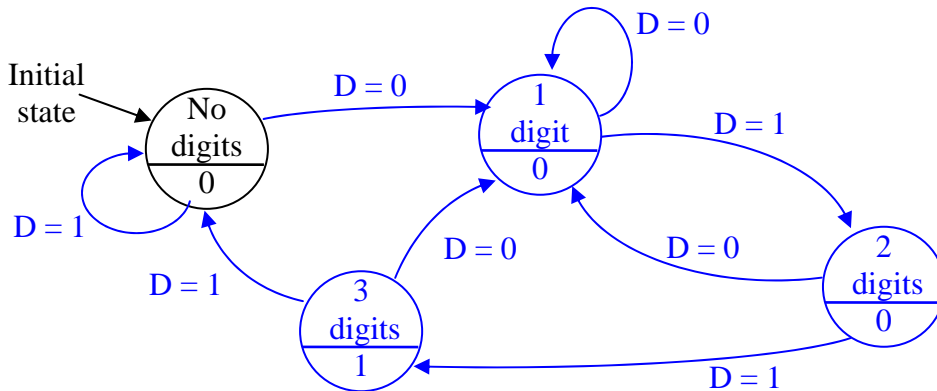


Longer answers – Points vary per problem

28. Make the state diagram that will output a '1' when the sequence '011' is detected in a serial stream of bits. For example, if the following binary stream is received:

0 0 1 0 1 1 1 0 1 0 0 1 0 1 1 0 0 0 1 1 0 1 1 0 1 1 1 0 0 1 0

then 1's will be output at these points. At all other times, the system will output zeros. Label the input D. (8 points)



29. Derive the minimum SOP expression from the Karnaugh map below. (6 points)

	<i>CD</i>			
	00	01	11	10
<i>AB</i>				
00	1	1	1	1
01	1	0	1	1
11	1	0	1	1
10	1	0	0	0

Red rectangle

A	B	C	D
0	0	0	0
0	0	0	1
0	0	1	1
0	0	1	0

C and D drop out.
Since both A and B
equal 0 for all cells,
they are inverted.

$$\bar{A} \cdot \bar{B}$$

Blue rectangle

A	B	C	D
0	0	0	0
0	1	0	0
1	1	0	0
1	0	0	0

A and B drop out.
Since both C and D
equal 0 for all cells,
they are inverted.

$$\bar{C} \cdot \bar{D}$$

Green rectangle

A	B	C	D
0	1	1	1
0	1	1	0
1	1	1	1
1	1	1	0

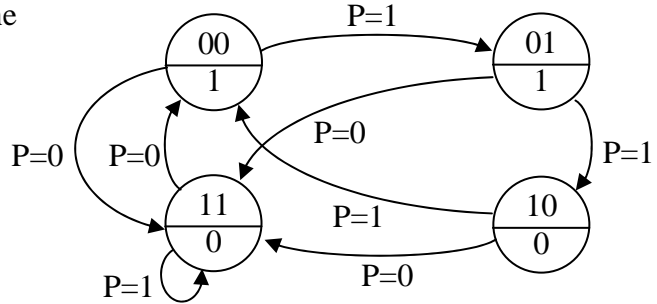
A and D drop out.
Since both B and C
equal 1 for all cells,
neither is inverted.

$$B \cdot C$$

The final answer is:

$$\bar{A} \cdot \bar{B} + \bar{C} \cdot \bar{D} + B \cdot C$$

30. Create the next state truth table and the output truth table for the state diagram to the right. Use the variable names S_1 and S_0 to represent the most significant and least significant bits respectively of the binary number identifying the state. Label the output 'X'. (8 points)



Next State T.T.

S_1	S_0	P	S_1'	S_0'
0	0	0	1	1
0	0	1	0	1
0	1	0	1	1
0	1	1	1	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Output T.T.

S_1	S_0	X
0	0	1
0	1	1
1	0	0
1	1	0

31. The three Boolean expressions below represent the *next state bits* (S_0' and S_1') and the *output bit* X based on the *current state* (S_0 and S_1) and the *input A*. Draw the logic circuit for the state machine including the latches and output circuitry. *Be sure to label the latch inputs and other signals.* (8 points)

$$S_0' = S_1 \cdot \bar{A}$$

$$S_1' = S_0 \cdot \bar{A}$$

$$X = S_1 + S_0$$

