

Points missed: \_\_\_\_\_ Student's Name: \_\_\_\_\_

Total score: \_\_\_\_\_/100 points

East Tennessee State University  
Department of Computer and Information Sciences  
CSCI 2150 (Tarnoff) – Computer Organization  
TEST 2 for Spring Semester, 2008

**Read this before starting!**

- The total possible score for this test is 100 points.
- This test is *closed book and closed notes*.
- *Please turn off all cell phones & pagers during the test.*
- **All answers must** be placed in space provided. Failure to do so may result in loss of points.
- **1 point** will be deducted per answer for missing or incorrect units when required. **No** assumptions will be made for hexadecimal versus decimal, so you should always include the base in your answer.
- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.
- *Calculators are not allowed.* Use the tables below for any conversions you may need. Leaving numeric equations is fine too.

Binary	Hex
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7

Binary	Hex
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Power of 2	Equals
$2^3$	8
$2^4$	16
$2^5$	32
$2^6$	64
$2^7$	128
$2^8$	256
$2^9$	512
$2^{10}$	1K
$2^{20}$	1M
$2^{30}$	1G

“Fine print”

Academic Misconduct:

Section 5.7 "Academic Misconduct" of the East Tennessee State University Faculty Handbook, June 1, 2001:

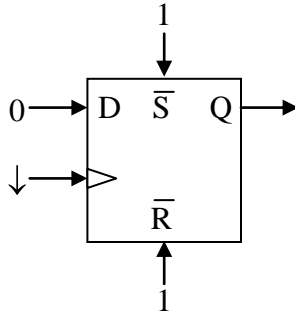
"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarizing, the changing or falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of 'F' on the work in question, a grade of 'F' of the course, reprimand, probation, suspension, and expulsion. For a second academic offense the penalty is permanent expulsion."

**Short answers – 2 points each unless otherwise noted**

For the following **three** circuits, identify the value of the output Q from the following choices. Consider the D-latch a **rising edge triggered latch**.

- a.) 1      b.) 0      c.)  $Q_0$  (stored value of Q)      d.) undefined/illegal      e.) can't tell

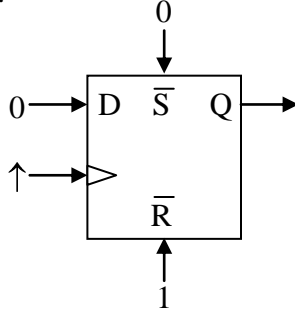
1.



Answer: c

First, neither the R-bar or S-bar lines are 0. Therefore, we can look at D and the clock to see what Q might be. Since the D-latch is rising edge triggered, and the input the clock is falling, not rising, then D has no effect on Q and Q is simply outputting the stored value of Q, i.e.,  $Q_0$ .

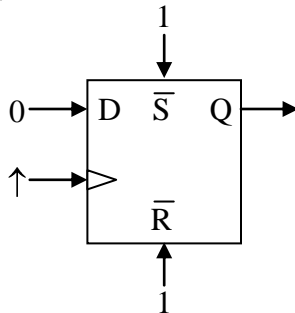
2.



Answer: a

The S-bar line is low which overrides any D or clock input. S-bar when asserted forces the output to equal 1. Therefore, the answer is a.

3.



Answer: b

First, neither the R-bar or S-bar lines are 0. Therefore, we can look at D and the clock to see what Q might be. Since the D-latch is rising edge triggered, and the input the clock is rising, then the value on D is being stored to Q and Q is outputting 0.

4. In the space below, write the product that represents the boolean expression for X in the truth table to the right.

There is only one row in the truth table with a 1 in it, which sounds a lot like the AND operation. (Which, by the way is what a product is, right?) To move the 1 from the bottom row where the AND operation would put it to the sixth row, we simply need to invert the necessary inputs so that the product will be a  $1 \cdot 1 \cdot 1$  when  $A=1$ ,  $B=0$ , and  $C=1$ . To do this, we need to invert B. Therefore, the product should be  $A \cdot \bar{B} \cdot C$ .

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

5. True or False: The  $\bar{S}$  and  $\bar{R}$  inputs of a D-latch override any input from the D and clock inputs.

6. What is the largest number of input variables a Karnaugh map can handle and still remain two dimensional?
- a.) 1    b.) 2    c.) 3    **d.) 4**    e.) 5    f.) 6    g.) there's no limit

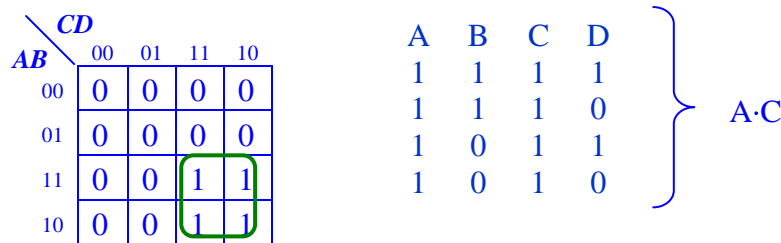
Each cell within a Karnaugh map must be adjacent to every other cell that differs by only one variable. Since each 2-dimensional cell has only 4 sides, then at most, a 2-D Karnaugh map can represent a 4-variable truth table. Adding another input will put us into the third dimension.

7. How many cells would a two-input Karnaugh Map have?
- a.) 2    **b.) 4**    c.) 6    d.) 8    e.) 12    f.) 16    g.) 32

Since a Karnaugh map must have a cell for every pattern of 1's and 0's for all of the inputs, and since a 2-input circuit has  $2^2 = 4$  possible combinations of 1's and 0's, then the answer is 4 cells.

8. In a 4-variable Karnaugh map, how many input variables (A, B, C, and/or D) does a single product have if its corresponding rectangle of 1's contains 4 cells?
- a.) 1    **b.) 2**    c.) 3    d.) Cannot be determined

The simplest way to answer this question is to create a 4-variable/input Karnaugh map that has a rectangle with four 1's, then figure out what the product is. The number of inputs in the product will give us our answer.

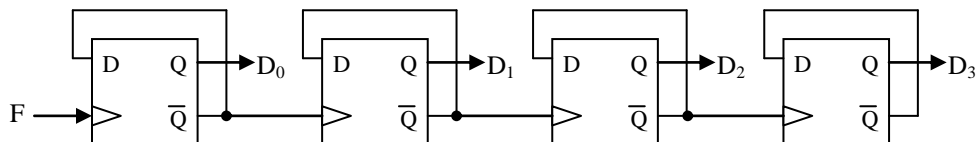


The resulting product has two inputs, A and C. You'll find that regardless of how the 4-cell rectangle is arranged, the resulting product will always have 2 inputs.

Another way of doing this is to realize that every time the size of a rectangle is doubled beyond the size of 1 cell, one variable drops out. For a four cell rectangle, the rectangle doubled twice, once for 1 to 2, then again for 2 to 4. This means of the 4 input variables, only 2 are left.

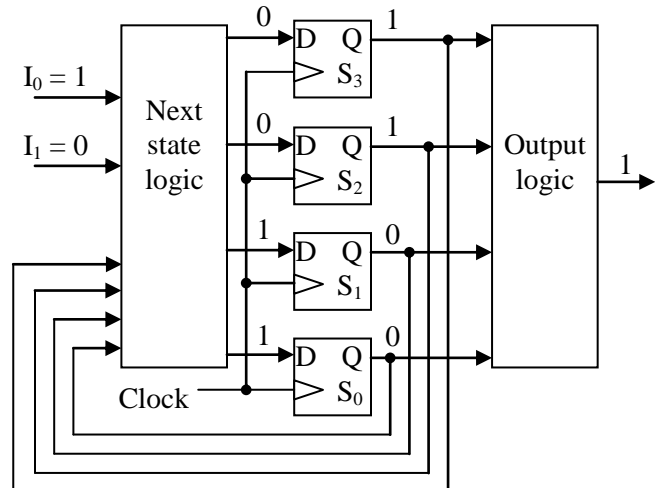
9. A falling edge triggered latch copies data from the D input to the Q output when the clock is:
- a.) a logic 0    **c.) changing from a 1 to a 0**    b.) a logic 1    d.) changing from a 0 to a 1
10. The cascaded divide-by-two circuits shown below can be used to \_\_\_\_\_ clock pulses. (There are actually two different answers that are acceptable.)

This circuit has two purposes. First, the final output, D<sub>3</sub>, has a clock frequency that is the frequency of F divided by 16. The combined outputs D<sub>3</sub>, D<sub>2</sub>, D<sub>1</sub>, and D<sub>0</sub> also can be used to count the number of clock pulses that have occurred on F.





The next six problems use the state machine circuit to the right. Assume that the states are numbered so that bit  $S_3$  is the most significant bit and bit  $S_0$  is the least significant bit.



12. What is the maximum number of states that this system can handle?

Since there are four latches, then the internal memory of this state machine can remember  $2^4 = 16$  states: 0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100, 1101, 1110, and 1111. Therefore, the answer is 16.

13. What is the current state of this system? Keep your answer in binary.

The current state is the value stored in the four latches and found at the Q outputs. In the case of the diagram above, that is 1100 with  $S_3$  being used as the most significant bit.

14. If the clock were to pulse right now, what would the next state be? Keep your answer in binary.

The next state is the value present at the D inputs, i.e., the value that would be stored if we had a clock pulse occur. In the case of the diagram above, that is 0011 with  $S_3'$  being the most significant bit.

$S_3$	$S_2$	$S_1$	$S_0$	X
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	1	0	0
1	1	1	1	1

15. The truth table to the right represents the output logic truth table for the above state machine. Circle the row that identifies the current output condition of the system, i.e., which row is represented by the current state of the logic in the diagram above without having any clock pulses occur?

The output is determined by the current state, i.e., 1100. Therefore, the thirteenth row identifies the output, which matches the 1 output from the figure.

16. If the clock were to pulse right now, what would the new output be? Use the truth table from the previous problem to answer the question.

- a.) 0      b.) 1      c.) Not enough information given

Since the next state is 0011, we go to the row in the truth table for 0011. This shows us that the output for the next state is 0.

17. How many rows would the next state logic truth table have for this circuit?

- a.)  $2^2 = 4$     b.)  $2^3 = 8$     c.)  $2^4 = 16$     d.)  $2^5 = 32$     **e.)  $2^6 = 64$**     f.)  $2^7 = 128$

Remember that the next state logic truth table depends on the current state (derived from  $S_3, S_2, S_1,$  and  $S_0$ ) and the current input ( $I_1$  and  $I_0$ ). This gives us 6 inputs. Since there are  $2^6 = 64$  combinations of 1's and 0's for 6 inputs, the answer is e. (Counting the arrows into the block labeled "Next state logic" would have also shown that there are 6 inputs to this logic.)

18. True or **False** Re-numbering the states of a state machine has no effect on the "next state" logic for the digital hardware implementation.

The numbering of the states directly affects the next state truth table, and therefore changes the logic that is derived from it. Therefore, the answer is **False**.

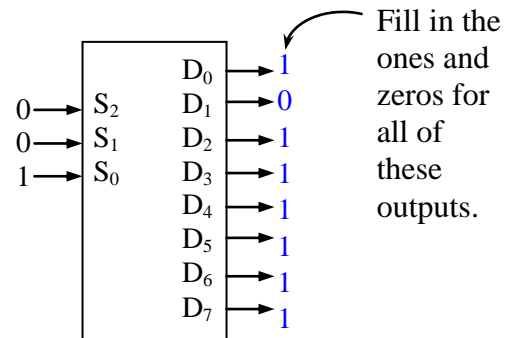
19. How many latches will a state machine with 25 states require?

- a.) 3    b.) 4    **c.) 5**    d.) 6    e.) 7    f.) 8    g.) 9

With 25 states, they would be numbered 0, 1, 2, 3, ... , and 24. Since  $24_{10} = 16_{10} + 8_{10} = 11000_2$ , a binary value with 5 bits, we will need 5 bits to represent the state. **Therefore, the answer is c.** Another way of looking at it is to see how many states it is possible to represent with n bits, and to figure out what value of  $2^n$  is greater than or equal to 24 different values.  $2^3 = 8$  which is not enough,  $2^4 = 16$  which is still not enough, but  $2^5 = 32$  which is more than enough. Therefore, 5 bits will do the trick.

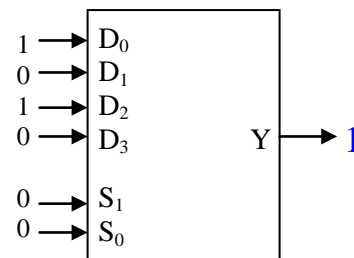
20. For the **active-low** output decoder shown to the right, fill in the values for all of the outputs  $D_0$  through  $D_7$ . Assume  $S_2$  is most significant bit of the inputs. (3 points)

Remember that the bits  $S_2, S_1,$  and  $S_0$  make up a digital selector with  $S_2$  being the most significant bit. The digital value of these three bits is 001 which when converted to decimal gives us 1. That means that output  $D_1$  is the selected output. Since it's active low, there will be a zero output on  $D_1$  and 1's everywhere else.

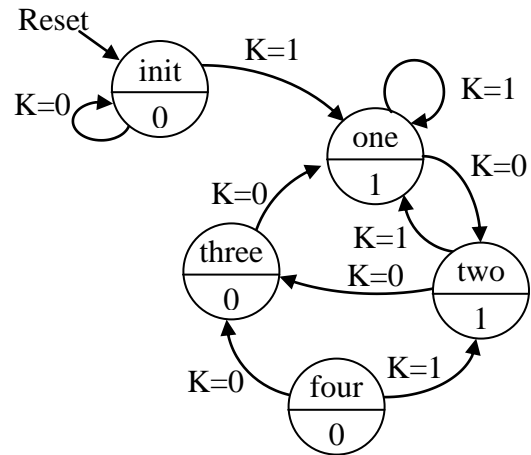


21. For the multiplexer/selector shown to the right, what is the output Y?

Similar to the previous problem, the output is "selected" by the selector inputs  $S_1$  and  $S_0$  with  $S_1$  being the most significant bit. The digital value of these two bits is  $00_2$  which equals a decimal 0. Therefore, the input  $D_0$  is going to be routed to the output Y making Y have an output of 1.



22. Identify the two errors in the state diagram to the right. The circuit is to have a single binary input K. Do not bother to correct the errors. (2 points for each error identified correctly)

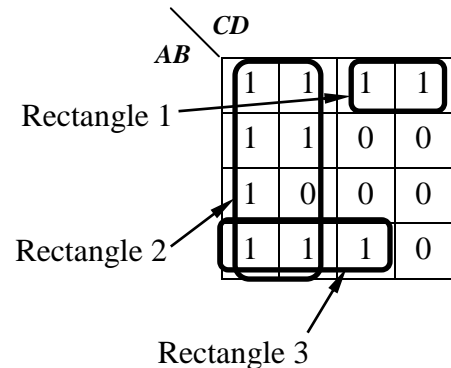


First of all, there is a "trick" here. Not really a nasty one, but if you're unfamiliar with state diagrams, one that might have fooled. It looks like there is no way to get to the "init" state. Actually, there is. It is entered during a reset, and like the fact that you should only see a Windows welcome screen once, it is okay to have states in our diagram that are only entered during a reset.

There is, however, a state that is unreachable even during a reset. That state is state "four". Notice that there are no arrows into state "four".

The second problem is that state "three" does not have a transition for K=1.

23. For the Karnaugh map to the right, identify three **problems** with how the rectangles have been made. Note that not all of the problems may be with a specific rectangle, but if there is a problem with a rectangle, be sure to identify it using the names given. (2 points each)



Problem 1: Rectangle 2 contains a zero.

Problem 2: Rectangle 3 contains three cells which is not a power of two.

Problem 3: Rectangle 1 isn't as large as it could be. It could cross the whole top row to include the two, topmost ones in Rectangle 2.

**Medium answers – 4 points each**

24. Complete the truth table to the right with the values for the sum-of-products expression

$$A \cdot \overline{B} + B \cdot \overline{C}$$

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Remember that each product generates a 1 when all of its inputs are one, e.g.,  $1 \cdot 1 \cdot 1 = 1$ . This means that if we can figure out where each product equals 1, we know where the 1's are in the truth table. The remaining positions are filled with zeros.

The first product,  $A \cdot \overline{B}$ , equals one when A=1 and B=0. Therefore, all rows where A=1 and B=0 should be set to 1.

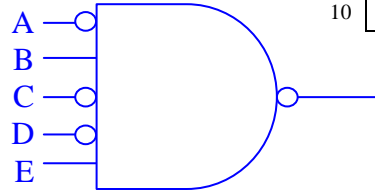
The second product,  $B \cdot \overline{C}$ , equals 1 when B=1 and when C=0. This happens in the third and seventh rows of the truth table. This gives us the pattern of 1's and 0's you see filled in above.

25. In the Karnaugh map to the right, draw the best pattern of rectangles you can. **Do not derive the SOP expression.**

Remember to only include X's in rectangles if they make the rectangle bigger. Do not include an X if it adds an additional rectangle.

	<b>CD</b>			
<b>AB</b>	00	01	11	10
00	1	1	0	0
01	0	1	1	0
11	0	1	X	1
10	0	0	X	0

26. In the space to the right, draw the decoding logic circuit with an active-low output that identifies when  $A = 0$ ,  $B = 1$ ,  $C = 0$ ,  $D = 0$ , and  $E = 1$ .

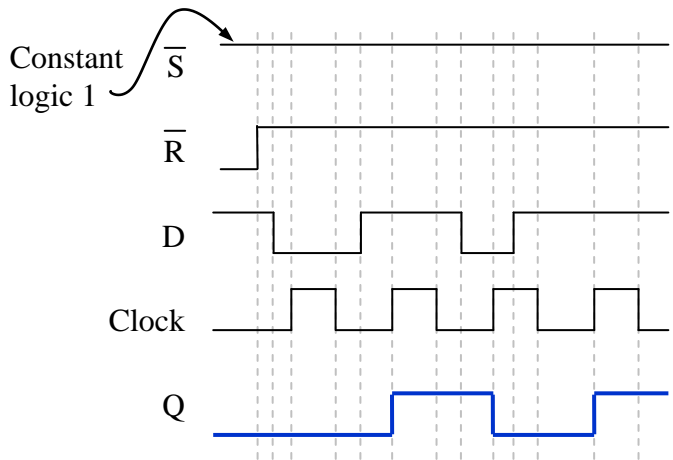
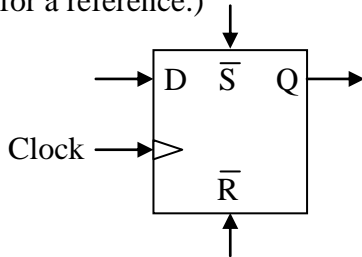


27. Create a Karnaugh map from the truth table below. **Do not worry about making the rectangles.**

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

	<b>C</b>	
<b>AB</b>	0	1
00	1	1
01	1	0
11	1	1
10	0	1

28. Show the D latch output waveform  $Q$  based on the inputs  $D$ ,  $\bar{S}$ ,  $\bar{R}$ , and clock indicated in the graph to the right. Assume the latch captures on the rising edge. (The figure below is just for a reference.)



First of all, since R-bar is 0 at the very beginning of the timing diagram, Q should start of as a 0. Once both S-bar and R-bar go high, then the rising edge of the clock will copy D to Q. The first time this happens, D is equal to zero, so although a 0 is copied to Q, Q doesn't appear to change since it was already set to 0. The rising edge of the second clock pulse stores a 1 from D to Q. The third clock pulse stores a 0 from D to Q. Finally, the fourth clock pulse stores another 1 to Q from D.

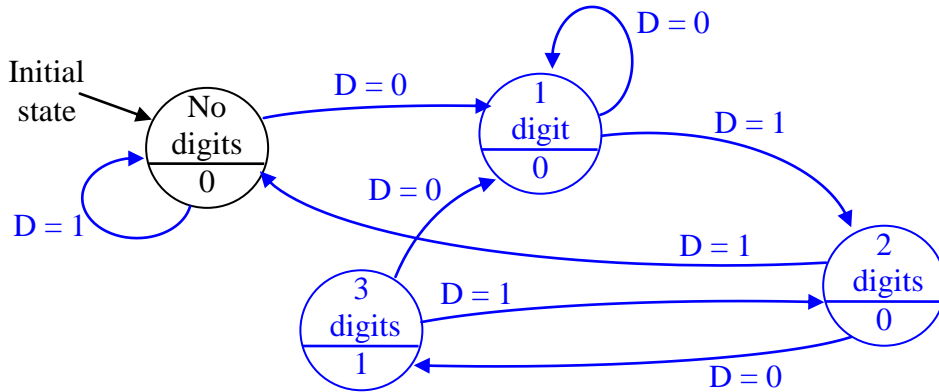


**Longer answers – Points vary per problem**

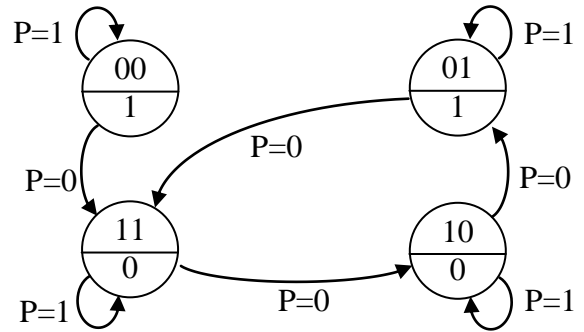
29. Make the state diagram that will output a '1' when the sequence '010' is detected in a serial stream of bits. For example, if the following binary stream is received:

1 0 1 0 1 1 1 0 1 0 1 0 0 1 1 0 0 0 1 1 1 1 0 0 1 0 0 0

then 1's will be output at these points. At all other times, the system will output zeros. **Label the input D.** (7 points)



30. Create the next state truth table and the output truth table for the state diagram to the right. The states have already been numbered. Use the variable names  $S_1$  and  $S_0$  to represent the most significant and least significant bits respectively of the binary number identifying the state. Label the output 'X'. (7 points)



Next State T.T.

$S_1$	$S_0$	P	$S_1'$	$S_0'$
0	0	0	1	1
0	0	1	0	0
0	1	0	1	1
0	1	1	0	1
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Output T.T.

$S_1$	$S_0$	X
0	0	1
0	1	1
1	0	0
1	1	0

31. Derive the minimum SOP expression from the Karnaugh map below. (6 points)

	<i>CD</i>			
	00	01	11	10
<i>AB</i>				
00	0	1	1	1
01	0	1	1	1
11	1	0	0	1
10	1	0	0	1

Red rectangle

A	B	C	D
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1

B and C drop out.  
 Since A=0, it should be inverted in the product. Since D=1, it isn't inverted.

$$\bar{A} \cdot D$$

Blue rectangle

A	B	C	D
0	0	1	0
0	1	1	0
1	1	1	0
1	0	1	0

A and B drop out.  
 Since C=1, it isn't inverted and since D=0, it is inverted.

$$C \cdot \bar{D}$$

Green rectangle

A	B	C	D
1	1	0	0
1	1	1	0
1	0	0	0
1	0	1	0

B and C drop out.  
 Since A=1, it isn't inverted. Since D=0, it is inverted.

$$A \cdot \bar{D}$$

The final answer is:

$$\bar{A} \cdot D + C \cdot \bar{D} + A \cdot \bar{D}$$

32. The three Boolean expressions below represent the *next state bits* ( $S_0'$  and  $S_1'$ ) and the *output bit X* based on the *current state* ( $S_0$  and  $S_1$ ) and the *input A*. Draw the logic circuit for the state machine including the latches and output circuitry. **Be sure to label the latch inputs and other signals.** (7 points)

$$S_0' = \bar{A} \cdot S_0$$

$$S_1' = A \cdot S_1$$

$$X = \bar{S}_1 + S_0$$

