Points missed: _____ Student's Name: _____

Total score: _____ /100 points

East Tennessee State University
Department of Computer and Information Sciences
CSCI 2150 (Tarnoff) – Computer Organization
TEST 2 for Spring Semester, 2009

Read this before starting!

- The total possible score for this test is 100 points.
- This test is ***closed book and closed notes.***
- ***Please turn off all cell phones & pagers during the test.***
- **All** answers **must** be placed in space provided. Failure to do so may result in loss of points.
- **1 point** will be deducted per answer for missing or incorrect units when required. **No** assumptions will be made for hexadecimal versus decimal, so you should always include the base in your answer.
- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.
- ***Calculators are not allowed.*** Use the tables below for any conversions you may need. Leaving numeric equations is fine too.

Binary	Hex
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7

Binary	Hex
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Power of 2	Equals
2^3	8
2^4	16
2^5	32
2^6	64
2^7	128
2^8	256
2^9	512
2^{10}	1K
2^{20}	1M
2^{30}	1G

"Fine print"

Academic Misconduct:

Section 5.7 "Academic Misconduct" of the East Tennessee State University Faculty Handbook, June 1, 2001:

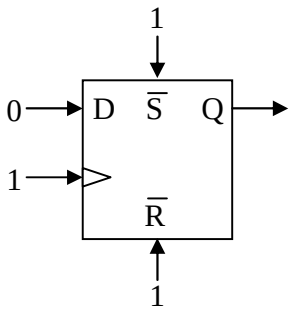
"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarism, the changing of falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of 'F' on the work in question, a grade of 'F' of the course, reprimand, probation, suspension, and expulsion. For a second academic offense the penalty is permanent expulsion."

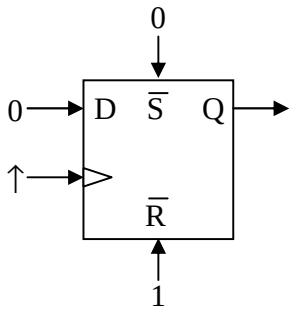
Short answers – 2 points each unless otherwise noted

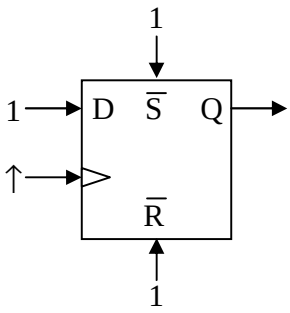
For each of the following ***three*** circuits, identify the value of the output Q from the following choices. Consider the D-latch a ***rising edge triggered latch***.

a.) 1 b.) 0 c.) Q_0 (stored value of Q) d.) undefined/illegal e.) can't tell

1. Answer: _____ 2. Answer: _____ 3. Answer: _____







4. Assume you have a truth table representing a circuit with four inputs, A, B, C, and D. How many rows in this truth table would have ones as a result of the expression $A \cdot \overline{B} \cdot \overline{D}$?

   a.) 2 b.) 4 c.) 6 d.) 8 e.) 12 f.) Cannot be determined

5. How many cells would a three-input Karnaugh Map have?

   a.) 2 b.) 4 c.) 6 d.) 8 e.) 12 f.) 16 g.) 32

6. True or False: The expression $(A+\overline{B})\cdot(\overline{A}+\overline{B}+C)$ is in proper product-of-sums format.

7. Create the sum that represents the truth table shown to the right. (3 points)

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

8. Create the product that represents the truth table shown to the right.

A	B	X
0	0	0
0	1	0
1	0	1
1	1	0

9. In a 4-variable Karnaugh map, how many input variables (A, B, C, and/or D) does a single product have if its corresponding rectangle of 1's contains 2 cells?

   a.) 1 b.) 2 c.) 3 d.) 4 e.) Cannot be determined

10. An falling-edge latch copies data from the D input to the Q output when the clock is:

    a.) a logic 0 b.) changing from a 1 to a 0 c.) a logic 1 d.) changing from a 0 to a 1

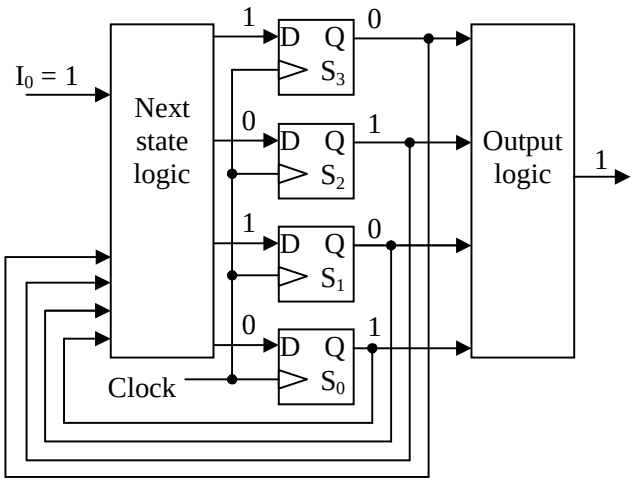
11. Which of the following expressions produces the truth table to the right?

a.) $A \cdot \overline{B} + \overline{C}$ b.) $A + \overline{C}$ c.) $A \cdot B + \overline{C}$

d.) $\overline{B} + A \cdot C$ e.) $A + \overline{B} \cdot C$ f.) $A + B \cdot \overline{C}$

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

The next six problems use the state machine circuit to the right. Assume that the states are numbered so that bit S_3 is the most significant bit and bit S_0 is the least significant bit.



12. What is the maximum number of states that this system can handle?

13. What is the current state of this system? Keep your answer in binary.

14. If the clock were to pulse right now, what would the next state be? Keep your answer in binary.

15. The truth table to the right represents the output logic truth table for the above state machine. Circle the row that identifies the current output condition of the system, i.e., which row is represented by the current state of the logic in the diagram above?

S_3	S_2	S_1	S_0	X
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

16. If the clock were to pulse right now, what would the new output be? Use the truth table from the previous problem to answer the question.

a.) 0 b.) 1 c.) Not enough information given

17. How many rows would the next state logic truth table have for this circuit?

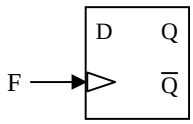
a.) $2^2 = 4$ b.) $2^3 = 8$ c.) $2^4 = 16$ d.) $2^5 = 32$ e.) $2^6 = 64$

18. True or False: Re-numbering the states of a state machine has no effect on the ***output logic*** for the digital hardware implementation.

19. How many latches will a state machine with 24 states require?

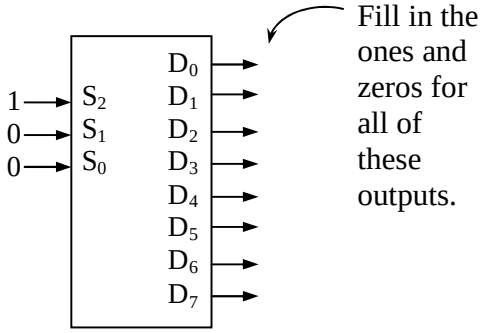
a.) 3 b.) 4 c.) 5 d.) 6 e.) 7 f.) 8 g.) 9

20. Make the connections to the latch in the figure to the right that makes a divide-by-two circuit, i.e., divides the frequency F in half at the output Q.

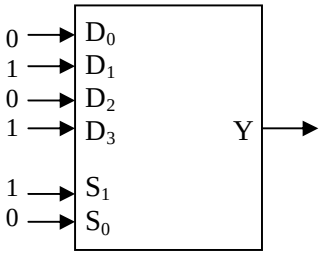


21. Two examples were given in class representing reasons why you would want to cascade multiple divide-by-two circuits. Name one of them.

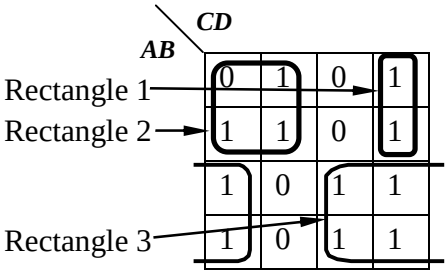
22. For the ***active-low*** output decoder shown to the right, fill in the values for all of the outputs D_0 through D_7. Assume S_2 is most significant bit of the inputs. (3 points)



23. For the multiplexer/selector shown to the right, what is the output Y?



24. For the Karnaugh map to the right, identify three ***problems*** with how the rectangles have been made. Note that not all of the problems may be with a specific rectangle, but if there is a problem with a rectangle, be sure to identify it using the names given. (2 points each)



Problem 1:

Problem 2:

Problem 3:

Medium answers – 4 points each

25. Complete the truth table to the right with the values for the following sum-of-products expression:

$$\overline{A} \cdot B + A \cdot \overline{C}$$

A	B	C	X
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

26. In the Karnaugh map to the right, draw the best pattern of rectangles you can. ***Do not derive the SOP expression.***

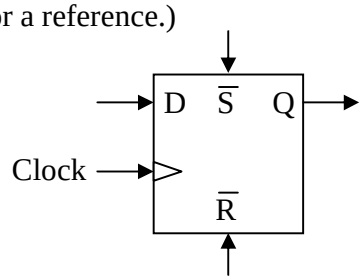
AB \ ***CD***	00	01	11	10
00	1	1	1	X
01	1	0	0	X
11	1	1	0	X
10	1	0	0	0

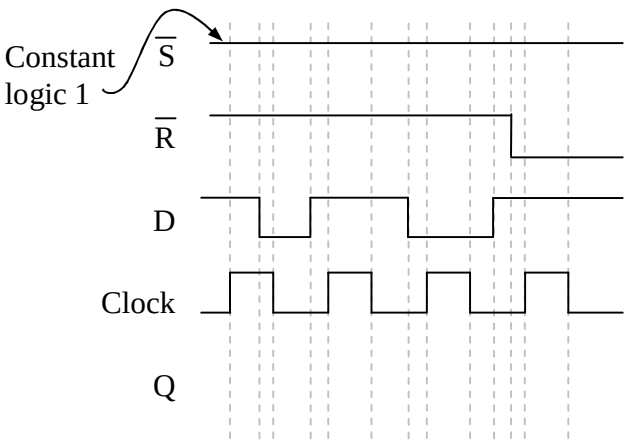
27. In the space to the right, draw the decoding logic circuit with an active-low output that identifies when A = 1, B = 1, C = 0, D = 1, and E = 1.

28. Create a Karnaugh map from the truth table below. ***Do not worry about making the rectangles.***

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	X

29. Show the *D* latch output waveform *Q* based on the inputs *D*, $\overline{S}$, $\overline{R}$, and clock indicated in the graph to the right. Assume the latch captures on the rising edge. (The figure below is just for a reference.)



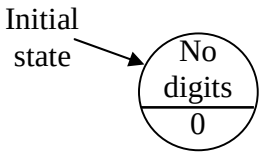


Longer answers – Points vary per problem

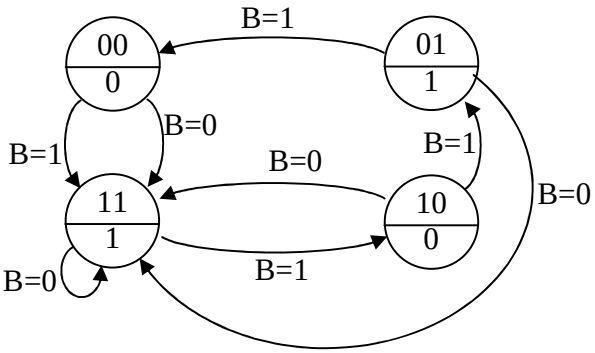
30. Make the state diagram that will output a '1' when the sequence '000' is detected in a serial stream of bits. For example, if the following binary stream is received:

1 0 1 0 1 1 1 0 1 0 0 0 0 1 1 0 0 0 1 1 0 1 0 0 0 1 1 0

then 1's will be output at these points. At all other times, the system will output zeros. Label the input D. (7 points)



31. Create the next state truth table and the output truth table for the state diagram to the right. The states have already been numbered. Use the variable names S_1 and S_0 to represent the most significant and least significant bits respectively of the binary number identifying the state. Label the output 'X'. (7 points)



32. Derive the minimum SOP expression from the Karnaugh map below. (6 points)

AB \ ***CD***	00	01	11	10
00	1	0	1	1
01	1	0	0	1
11	0	0	0	1
10	0	0	0	1

33. The three Boolean expressions below represent the ***next state bits (S_0' and S_1')*** and the ***output bit X*** based on the ***current state (S_0 and S_1)*** and the ***input A***. Draw the logic circuit for the state machine including the latches and output circuitry. ***Be sure to label the latch inputs and other signals.*** (6 points)

$S_0' = A \cdot S_1$ $\qquad$ $S_1' = \overline{A} \cdot S_0$ $\qquad$ $X = S_1 + S_0$