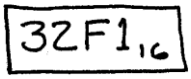
Points missed: _____ Student's Name: _____

Total score: _____ /100 points

East Tennessee State University
Department of Computer and Information Sciences
CSCI 4717 – Computer Architecture
TEST 1 for Fall Semester, 2007
Section 001

Read this before starting!

- The total possible score for this test is 100 points.
- This test is ***closed book and closed notes***
- ***Please turn off all cell phones & pagers during the test.***
- You may use one sheet of scrap paper that you will turn in with your test.
- **When possible, indicate final answers by drawing a box around them. This is to aid the grader. Failure to do so might result in no credit for answer. Example:**



- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.

Binary	Hex
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7

Binary	Hex
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Power of 2	Equals
2^4	16
2^5	32
2^6	64
2^7	128
2^8	256
2^9	512
2^{10}	1K
2^{20}	1M
2^{30}	1G

"Fine print"

Academic Misconduct:

Section 5.7 "Academic Misconduct" of the East Tennessee State University Faculty Handbook, June 1, 2001:

"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarism, the changing of falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of 'F' on the work in question, a grade of 'F' of the course, reprimand, probation, suspension, and expulsion. For a second academic offense the penalty is permanent expulsion."

1. If ***security*** is a critical performance measure for a component of a system design, which would you rather implement the component in, hardware, firmware, or software? In a sentence or two, justify your answer. (2 points)

2. Which method of component implementation is the cheapest to manufacture, hardware, firmware, or software? (2 points)

   a.) Hardware b.) Firmware c.) Software

3. For the following items, indicate whether the characteristic more closely describes a top-down (TD) or a bottom-up (BU) design method. (1 point each)

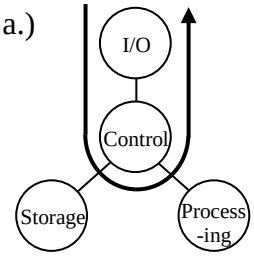
   ____ You're under a time crunch to get a project done quickly

   ____ The design needs to precisely follow existing industrial standards

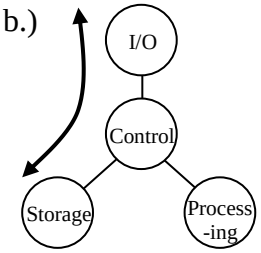
   ____ There are critical performance goals that need to be met

For the following 3 problems, identify which of the following system functional diagrams, a, b, c, or d, best describes the operation of the example system or application. Note: Focus only on the immediate system described. Do not include external components such as devices across a network that may work with the system. (2 points each)

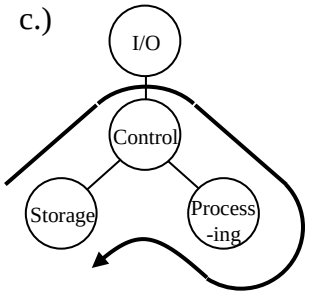
a.)



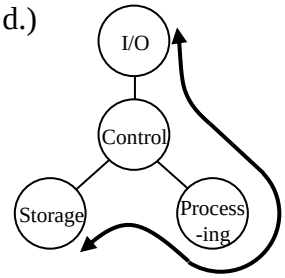
b.)



c.)



d.)



4. A kiosk that simply displays information sent to it from across a network: _____

5. An encoder converting raw stored video to MPEG then storing it back to the hard drive: _____

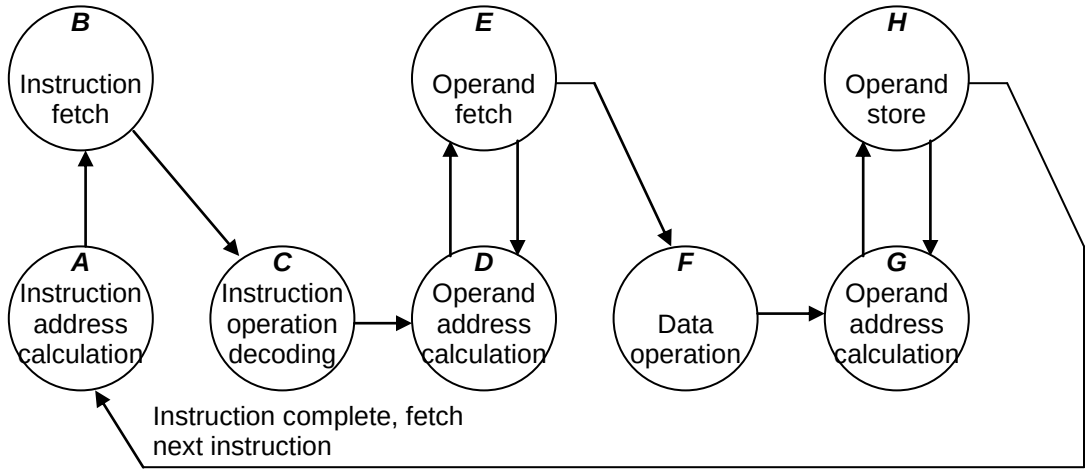
6. An encoder converting raw live video to MPEG then storing it to the hard drive: _____

7. Name three of the five effects discussed in class that Moore's law has had on the contemporary application of computers. (4 points)

8. Circle ***all*** of the following traits that are identified as key concepts of the von Neumann architecture. (3 points)

   a.) Control unit interprets instructions and causes them to be executed
   b.) Execution of instructions is performed in a 2-stage pipeline
   c.) Sequential execution of code except in the case of "jumps"
   d.) Input/output is served through the use of interrupts
   e.) Both data and instructions stored in a common main memory

Use the figure of the instruction cycle state diagram below to answer the following 3 questions.



9. List by letter (A, B, C, D, E, F, G, and/or H) the states that may have to be executed multiple times for a single instruction. (3 points)

10. List by letter the state or states whose duration (time) may vary depending on the instruction. (3 points)

11. Assuming a system supports interrupts, list by letter the state or states after which the system will check to see if an interrupt has occurred. (2 points)

12. ***Name and justify*** the ***two*** most important performance aspects of a missile guidance system. (3 points)

13. How does the processor keep track of (store) the previous register values and instruction pointer for the code currently being executed before servicing an interrupt? (2 points)

14. Give an example of a specific device that uses the ***direct method*** for accessing memory? (2 points)

15. Assume that a new data storage technology has been developed that needs to be inserted somewhere in the memory hierarchy. Which characteristic is more important in determining where it is placed in the hierarchy, access time, capacity, or volatility? (2 points)

    a.) Access time b.) Capacity c.) Volatility

The following table represents 12 lines of a 4-way set associative cache, i.e., there are four lines per set, three sets of which are showing. Notice that the set ID values start at 101101101_2 and increment every fourth. This is meant to imply that you are looking at a very small group of lines/sets within the cache. There are 12 bits for the tag, 9 bits for the set id, and 3 bits for the word id. Answer the following 2 questions based on this cache.

Tag (binary values)	Set ID (binary values)	Word within block							
		000	001	010	011	100	101	110	111
100001001001	101101101	FF_{16}	$1F_{16}$	$5B_{16}$	$9A_{16}$	00_{16}	61_{16}	$C2_{16}$	23_{16}
100001100100	101101101	EF_{16}	$0F_{16}$	$4B_{16}$	$8A_{16}$	10_{16}	71_{16}	$D2_{16}$	33_{16}
101011010110	101101101	DF_{16}	FB_{16}	$3B_{16}$	$7A_{16}$	20_{16}	81_{16}	$E2_{16}$	43_{16}
100101101011	101101101	CF_{16}	EB_{16}	$2B_{16}$	$6A_{16}$	30_{16}	91_{16}	$F2_{16}$	53_{16}
110110110100	101101110	BF_{16}	DB_{16}	$1B_{16}$	$5A_{16}$	40_{16}	$A1_{16}$	02_{16}	63_{16}
100111010101	101101110	AF_{16}	CB_{16}	$0B_{16}$	$4A_{16}$	50_{16}	$B1_{16}$	12_{16}	73_{16}
101010111110	101101110	$7F_{16}$	BB_{16}	FA_{16}	$3A_{16}$	84_{16}	$E5_{16}$	46_{16}	$A7_{16}$
101010010011	101101110	$6F_{16}$	AB_{16}	EA_{16}	$2A_{16}$	94_{16}	$F5_{16}$	56_{16}	$B7_{16}$
011101001000	101101111	$5F_{16}$	$9B_{16}$	DA_{16}	$1A_{16}$	$A4_{16}$	$A5_{16}$	66_{16}	$C7_{16}$
000011101101	101101111	$4F_{16}$	$8B_{16}$	CA_{16}	$0A_{16}$	$B4_{16}$	15_{16}	76_{16}	$D7_{16}$
010110110010	101101111	$3F_{16}$	$7B_{16}$	BA_{16}	$F9_{16}$	$C4_{16}$	25_{16}	86_{16}	$E7_{16}$
101011111011	101101111	$2F_{16}$	$6B_{16}$	AA_{16}	$E9_{16}$	$D4_{16}$	35_{16}	96_{16}	$F7_{16}$

16. A copy of the data from memory address 96BB6A (hex) is contained in the portion of the cache shown above. Enter the value that was retrieved from that address in the space below as a two-digit hexadecimal number. (3 points)

17. How many ***lines*** are contained in this cache? (2 points)

18. Which cache mapping function allows a block from memory to be stored in any line of the cache? (2 points)

    a.) Direct mapping b.) Set associative mapping c.) Fully associative mapping

19. Which cache mapping function does not require a replacement algorithm? (2 points)

    a.) Direct mapping b.) Set associative mapping c.) Fully associative mapping

20. Assume a memory access to main memory on a cache "miss" takes 20 ns and a memory access to the cache on a cache "hit" takes 4 ns. If 75% of the processor's memory requests result in a cache "hit", what is the average memory access time? Show your work if you are worried about your math. (2 points)

    a.) 3 nS b.) 4 nS c.) 6 nS d.) 10 nS e.) 20 nS f.) 24 nS

21. Which cache write mechanism creates more bus traffic? (2 points)

    a.) Write through b.) Write back

22. Which cache write mechanism allows an updated memory location in the cache to remain out of date in memory until the block containing the updated memory location is replaced in the cache? (2 points)

    a.) Write through b.) Write back c.) Both d.) Neither

23. What is the simplest solution to prevent problems with a multiprocessor/cache system from having invalid data in one of the caches? Hint: it isn't write through or write back and it's not very efficient. (2 points)

24. True or false: Like the memory hierarchy, the mezzanine bus structure places the faster busses closer to the processor. (2 points)

25. Give an example of a device that would be attached to the processor's local bus. In the Pentium organization, this would be between the Northbridge and the processor. (2 points)

26. List two of the three problems discussed in class that occur when the number of devices on a single bus increases. (3 points)

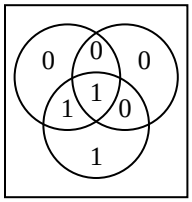
27. Give an example of a device that would be well-suited to an x32 PCI-E slot. (2 points)

28. Of the following characteristics, identify by placing a checkmark in the appropriate column whether the characteristic describes PCI, PCI-X, and/or PCI-E. Some rows (characteristics) will have more than one checkmark. (Each row is worth 1 point)

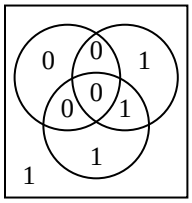
Characteristic	PCI	PCI-X	PCI-E
Transmits data and control serially	☐	☐	☐
Uses differential signalling similar to Manchester encoding to allow for long distance communication	☐	☐	☐
Supports the PCI command structure making it compatible with legacy software. (Check one or both)		☐	☐

29. What is the purpose of bus arbitration? (3 points)

30. The graphic to the right depicts the digits of a 4-bit Hamming code where a single bit error has occurred. Circle the bit that has flipped. (2 points)



31. True or false: The graphic to the right depicts the digits of a 4-bit Hamming code with parity where a double bit error has occurred. (2 points)



32. How many check code (parity) bits would you need to provide single error correction for 48 data bits? (2 points)

a.) 2 b.) 3 c.) 4 d.) 5 e.) 6 f.) 7 g.) 8 h.) 9 i.) 10

33. Which DRAM technology overlaps data read with column address write for next read, i.e., they happen simultaneously? (2 points)

a.) Fast Page Mode b.) Extended Data Out c.) Both

34. Which DRAM technology uses fixed row address for multiple column reads? (2 points)

a.) Fast Page Mode b.) Extended Data Out c.) Both

35. The table below describes the position number of the data and code bits of a single error correction code for eight data bits D_7, D_6, D_5, D_4, D_3, D_2, D_1, and D_0. Determine the equations to derive P_3, P_2, P_1, and P_0 from D_0 through D_7. (4 points)

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Position number	1111	1110	1101	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001
Data bit	not used	not used	D_7	D_6	D_5	D_4	D_3		D_2	D_1	D_0		not used		
Check code bit								P_3				P_2		P_1	P_0

P_3 =

P_2 =

P_1 =

P_0 =

36. For the error correcting system of the previous question, assume that the check code ***retrieved*** from memory was 0101 and the newly ***calculated*** check code on the data retrieved from memory was 1110. Assuming a single bit error has occurred, which bit was the one that flipped, D_7, D_6, D_5, D_4, D_3, D_2, D_1, D_0, P_3, P_2, P_1, or P_0? (2 points)

37. The translation lookaside buffer (TLB) is basically a cache for page tables. A TLB "miss" is a request for a page that isn't in the TLB. Name one way that we can reduce the chances of a TLB miss. (3 points)

38. Using paging with 10 processes and a page size of 4K (4096) words, what is the most memory that is wasted? (2 points)

39. What problem is caused by small pages in virtual memory? (2 points)

40. True or false: In virtual memory, the size of a page in a program's logical space is the same as the size of a frame in the physical memory space. (2 points)

41. Of the following characteristics, identify by placing a checkmark in the appropriate column whether the characteristic describes an inverted page table or a translation lookaside buffer. (Each row is worth 1 point)

Characteristic	Inverted Page Table	Translation Lookaside Buffer
Size is based on number of frames in memory rather than number of pages in program's logical space.	☐	☐
Acts like a cache for the most recently used entries of a page table.	☐	☐
Uses a hashing algorithm combined with a linked list to locate page table entries	☐	☐

42. Using the page table shown to the right representing a specific process, calculate the physical address from the logical address $62A3_{16}$. Assume a page size of $2^{12} = 4096$ words. The values in the page table are in hexadecimal. Be sure to show your work for partial credit. (3 points)