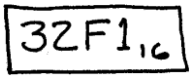
Points missed: _____ Student's Name: _____

Total score: _____ /100 points

East Tennessee State University
Department of Computer and Information Sciences
CSCI 4717 – Computer Architecture
TEST 3 for Fall Semester, 2006

Read this before starting!

- The total possible score for this test is 100 points.
- This test is ***closed book and closed notes***
- ***Please turn off all cell phones & pagers during the test.***
- You may use one sheet of scrap paper that you will turn in with your test.
- **When possible, indicate final answers by drawing a box around them. This is to aid the grader (who might not be me!) Failure to do so might result in no credit for answer. Example:**



- **1 point will be deducted** per answer for missing or incorrect units when required. **No** assumptions will be made for hexadecimal versus decimal, so you should always include the base in your answer.
- If you perform work on the back of a page in this test, indicate that you have done so in case the need arises for partial credit to be determined.

"Fine print"

Academic Misconduct:
Section 5.7 "Academic Misconduct" of the East Tennessee State University Faculty Handbook, October 21, 2005:

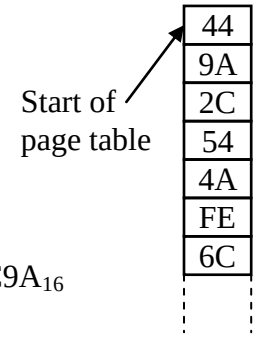
"Academic misconduct will be subject to disciplinary action. Any act of dishonesty in academic work constitutes academic misconduct. This includes plagiarism, the changing of falsifying of any academic documents or materials, cheating, and the giving or receiving of unauthorized aid in tests, examinations, or other assigned school work. Penalties for academic misconduct will vary with the seriousness of the offense and may include, but are not limited to: a grade of 'F' on the work in question, a grade of 'F' of the course, reprimand, probation, suspension, and expulsion. For a second academic offense the penalty is permanent expulsion."

1. True or false: A page fault always results in a page being removed from memory to make room for a new page. (2 points)
2. True or false: In a system that uses paging where processes are divided into pages, all pages except for the last page of a process are equal sizes. (2 points)
3. True or false: In a system that uses paging, the process page size is equal to the memory page frame size. (2 points)
4. True or false: In a system that uses paging, the pages of a process must be in order in memory. (2 points)
5. True or false: In a system that uses paging, the pages of a process must be in contiguous (adjacent or unbroken) memory. (2 points)
6. In a system that uses paging, _____ maintains a list of the free frames. (2 points)

   a.) the applications or processes
   b.) a hardware mechanism in main memory
   c.) a hardware mechanism in the cache
   d.) the operating system
   e.) none of the above

7. What problem is typically caused by large virtual memory page sizes? (2 points)

8. Using the page table shown to the right representing a specific process, calculate the physical address from the logical address $079A_{16}$. Assume a page size of $2^8 = 256$. (3 points)



   a.) $9A_{16}$ b.) $79A_{16}$ c.) $449A_{16}$ d.) $FE9A_{16}$ e.) $6C9A_{16}$
   f.) $9A9A_{16}$ g.) Not enough of the page table given to calculate

9. Assume the page size of the previous problem changes to $2^9 = 512$, but everything else remains the same. What is the physical address from the logical address $079A_{16}$. (3 points)

   a.) $39A_{16}$ b.) $79A_{16}$ c.) $559A_{16}$ d.) $549A_{16}$ e.) $6C9A_{16}$
   f.) $A99A_{16}$ g.) Not enough of the page table given to calculate h.) None of the above

10. A(n) _____ saves the memory required for a page table by maintaining a table of only the pages represented by real memory and ***not*** all of the pages for a process. (2 points)

    a.) translation lookaside buffer b.) virtual page table c.) segmentation table
    d.) partition table e.) inverted page table f.) none of the above

11. The single instruction below is a three-operand instruction. In the table below, write three short programs that do exactly the same thing, one with two-operand instructions, one with one-operand instructions, and one with zero-operand instructions. If it fits the need of the instruction, feel free to use register names R1, R2, etc. (5 points)

```
MULT A,B,C          ;A = B × C
```

Two operand instructions	***One operand instructions***	***Zero operand instructions***

12. Which of the following operations is performed by the zero-operand assembly language code shown to the right? (2 points)

```
PUSH A
PUSH B
MULT
PUSH C
ADD
PUSH D
PUSH E
SUB
MULT
POP Y
```

a.) $Y = ((B \times C) + D) \times (A - E)$
b.) $Y = A \times (B \times (C + D) - E)$
c.) $Y = (A \times (B + C)) \times (D - E)$
d.) $Y = ((A \times B) + C) \times (D - E)$
e.) $Y = (A + (B \times C) - D) \times E$
f.) None of the above

13. From the list below of stages of a 6-stage pipeline, identify the stage at which the outcome of a conditional branch has been determined. Circle one. (2 points)

a.) Fetch instruction (FI) b.) Decode instruction (DI) c.) Calculate operands (CO)
d.) Fetch operands (FO) e.) Execute Instruction (EI) f.) Write Operand (WO)

14. From the list below of stages of a 6-stage pipeline, identify all of the stage(s) that may vary considerably in duration depending on the instruction or operand. Circle all that apply. (2 points)

a.) Fetch instruction (FI) b.) Decode instruction (DI) c.) Calculate operands (CO)
d.) Fetch operands (FO) e.) Execute Instruction (EI) f.) Write Operand (WO)

15. From the list below of stages of a 6-stage pipeline, identify all of the stages that are ***always*** used in the execution of all instructions. Circle all that apply. (2 points)

a.) Fetch instruction (FI) b.) Decode instruction (DI) c.) Calculate operands (CO)
d.) Fetch operands (FO) e.) Execute Instruction (EI) f.) Write Operand (WO)

16. From the list below of stages of a 6-stage pipeline, identify the stage after which the processor check for interrupts? Circle one. (2 points)

a.) Fetch instruction (FI) b.) Decode instruction (DI) c.) Calculate operands (CO)
d.) Fetch operands (FO) e.) Execute Instruction (EI) f.) Write Operand (WO)

17. An instruction prefetch architecture is essentially a _____- stage pipeline. (2 points)

    a.) 1 b.) 2 c.) 3 d.) 4 e.) 5 f.) 6 g.) 7

18. In an ideal implementation, what is the speed up of a processor with a *k*-stage pipeline over a non-pipelined processor if the duration of each stage is τ? Don't consider pipeline flushes or delays incurred between stages. (2 points)

    a.) $k \cdot \tau$ b.) $k-2$ c.) $k-1$ d.) k e.) $(k+1) \cdot \tau$ f.) $k+\tau-1$ g.) none of the above

19. How many bits are required for each conditional branch in a branch history table in order to remember the past 2 branch outcomes for a specific instruction? (2 points)

    a.) 2 b.) 3 c.) 4 d.) 5 e.) 6 f.) 7 g.) 8

20. List two of the three causes discussed in class of disrupting a pipeline. (3 points)

For problems 21, 22, and 23, consider the following section of code.

```
for (i=0; i<2; i++)
{
     for (j=0; j<5; j++)
     {
          for (k=0; k<4; k++)
               sum += array_val[i, j, k];
     }
}
```

21. Once compiled, how many conditional jumps would be contained in the machine code resulting from the above section of code, i.e., static occurrence? (2 points)

22. After fully executing the above section of code, how many conditional jumps would the CPU have encountered, i.e., dynamic occurrence? (2 points)

23. Using the static branch prediction algorithm "branch always," how many of the conditional jumps calculated in the previous problem would have been predicted ***incorrectly***? (2 points)

24. There are 3 types of static branch prediction methods: predict always taken, predict never taken,

    and _____ (fill in the blank) (2 points)

25. For the six architectural characteristics listed below, identify whether the statement more closely identifies a CISC architecture or a RISC architecture. (6 points)

CISC	RISC	
☐	☐	Assembly language is closer to high-level language
☐	☐	Tends to have fewer stages in pipeline
☐	☐	Tends to have fewer addressing modes
☐	☐	Allows for indirect addressing
☐	☐	Registers tend to be more specialized than general purpose
☐	☐	Allows the operands of an arithmetic instruction to be memory references

26. What is the absolute minimum number of registers required to execute the code below. (2 points)

a.) 2 b.) 3 c.) 4 d.) 5 e.) 6 f.) 7 g.) 8

```
int done = 0;
int user_input << cin;
while (!done)
{
   int calc = 0;
   switch (user_input)
   {
      case 0:
         for (int i=0; i<5; i++) calc = (calc << 1) + i;
         break;
      case 1:
         for (int j=0; j<10; j++) calc = (calc << 1) + j;
         break;
      default:
         calc = 7;
         done = 1;
         break;
   }
   for (int k=0; k<calc; k++) cout << ".";
}
```

27. True or false: The purpose behind the delayed branch is to avoid flushing the pipeline. (2 points)

28. True or false: The purpose behind the delayed load is to avoid flushing the pipeline. (2 points)

29. After which line in the code below does a NOP need to be inserted to provide a ***delayed load*** to avoid a problem with a data dependency? (2 points)

a.) L1 b.) L2 c.) L3 d.) L4 e.) L5 f.) L6

```
L1:     mov    al,[1000h]        ;Load al w/value from memory
L2:     mov    ah,[1001h]        ;Load ah w/value from memory
L3:     add    ah,al             ;ah += al
L4:     dec    al                ;al--
L5:     bne    L3                ;Branch if al is not equal to 0
L6:     mov    [1002h],ah        ;Store ah to memory
```

30. Identify the write-read, write-write, and read-write dependencies in the instruction sequence below by entering each line pair with a dependency in the correct column of the table to the right. For example, if L1 and L4 had a write-write dependency (which they don't), you would enter L1-L4 in the column labeled "write-write". (4 points)

```
L1: R3 = R2 + R5
L2: R3 = R3 + 16
L3: R3 = R3 + R5
L4: R5 = R1 - R2
L5: R1 = R3 + 32
```

write-read	write-write	read-write

For problems 31, 32, and 33, use the figure to the right which represents the execution of 6 instructions on an "in-order-issue/in-order-completion" machine.

Assume that there is only one data dependency in the sequence, a true data dependency (write-read) between I1 and I4, i.e., I4 depends on the completion of I1 before it can execute. As for resource dependencies, assume that any instructions that share a column in the execute stage require the same resource.

Decode		Execute			Write		Cycle
I1	I2						1
	I2	I1					2
I3	I4	I1					3
I3	I4	I2					4
I5	I6		I4	I3	I1	I2	5
I5	I6			I3			6
		I5	I6		I3	I4	7
					I5	I6	8

31. In an out-of-order-issue/out-of-order-completion architecture, what is the earliest cycle I4 could enter the execute stage? (2 points)

a.) 1 b.) 2 c.) 3 d.) 4 e.) 5 f.) 6 f.) 7 g.) 8

32. In an out-of-order-issue/out-of-order-completion architecture, what is the earliest cycle I5 could enter the execute stage? (2 points)

a.) 1 b.) 2 c.) 3 d.) 4 e.) 5 f.) 6 f.) 7 g.) 8

33. In an out-of-order-issue/out-of-order-completion architecture, what is the earliest cycle I3 could enter the execute stage? (2 points)

a.) 1 b.) 2 c.) 3 d.) 4 e.) 5 f.) 6 f.) 7 g.) 8

34. Multiple Instruction/Multiple Data Stream architectures are referred to as tightly coupled when: (2 points)

a.) they communicate over a local area network (LAN)
b.) the network they are on is dedicated to the system, i.e., there is no other traffic
c.) they share a single hard drive or RAID for storage across a network
d.) they communicate through a shared memory
e.) none of the above

35. Which Multiple Instruction/Multiple Data Stream architecture is better suited to processes that require a high level of interaction, loosely coupled or tightly coupled? (2 points)

a.) loosely coupled b.) tightly coupled

36. A cluster is an example of: (2 points)

a.) a single instruction/single data stream architecture
b.) a single instruction/multiple data stream architecture
c.) a multiple instruction/single data stream architecture
d.) a tightly coupled multiple instruction/multiple data stream architecture
e.) a loosely coupled multiple instruction/multiple data stream architecture

37. Assume a multiprocessor system uses the MESI protocol. If the current state of a line in processor A's cache is ***modified***, do valid copies of the data exist in other caches? (2 points)

a.) yes b.) no c.) cannot tell

38. Assume a multiprocessor system uses the MESI protocol. If the current state of a line in processor A's cache is ***exclusive***, do valid copies of the data exist in other caches? (2 points)

a.) yes b.) no c.) cannot tell

39. Assume a multiprocessor system uses the MESI protocol. If the current state of a line in processor A's cache is exclusive and processor B loads the same line into its cache, what is the new state of that line in processor A's cache? (2 points)

a.) modified b.) exclusive c.) shared d.) invalid e.) cannot be determined

40. Which SMP bus configuration is simplest due to its architecture being closest to the single-processor architecture? (2 points)

a.) time-shared bus b.) multiport memory c.) central controller

41. Which SMP bus configuration is most reliable due to the fact that there is no central point of failure? (2 points)

a.) time-shared bus b.) multiport memory c.) central controller

42. The snoopy protocol is more suited to the _____ interconnection method for symmetric multiprocessors. (2 points)

a.) time-shared bus b.) multiport memory c.) central controller

43. For the four characteristics listed below, identify whether the statement more closely identifies an SMP system or a cluster. (4 points)

SMP	Cluster	
☐	☐	Operation is closer to that of a single processor system
☐	☐	Easier to upgrade incrementally
☐	☐	Lower overall power consumption
☐	☐	Older, more established track record